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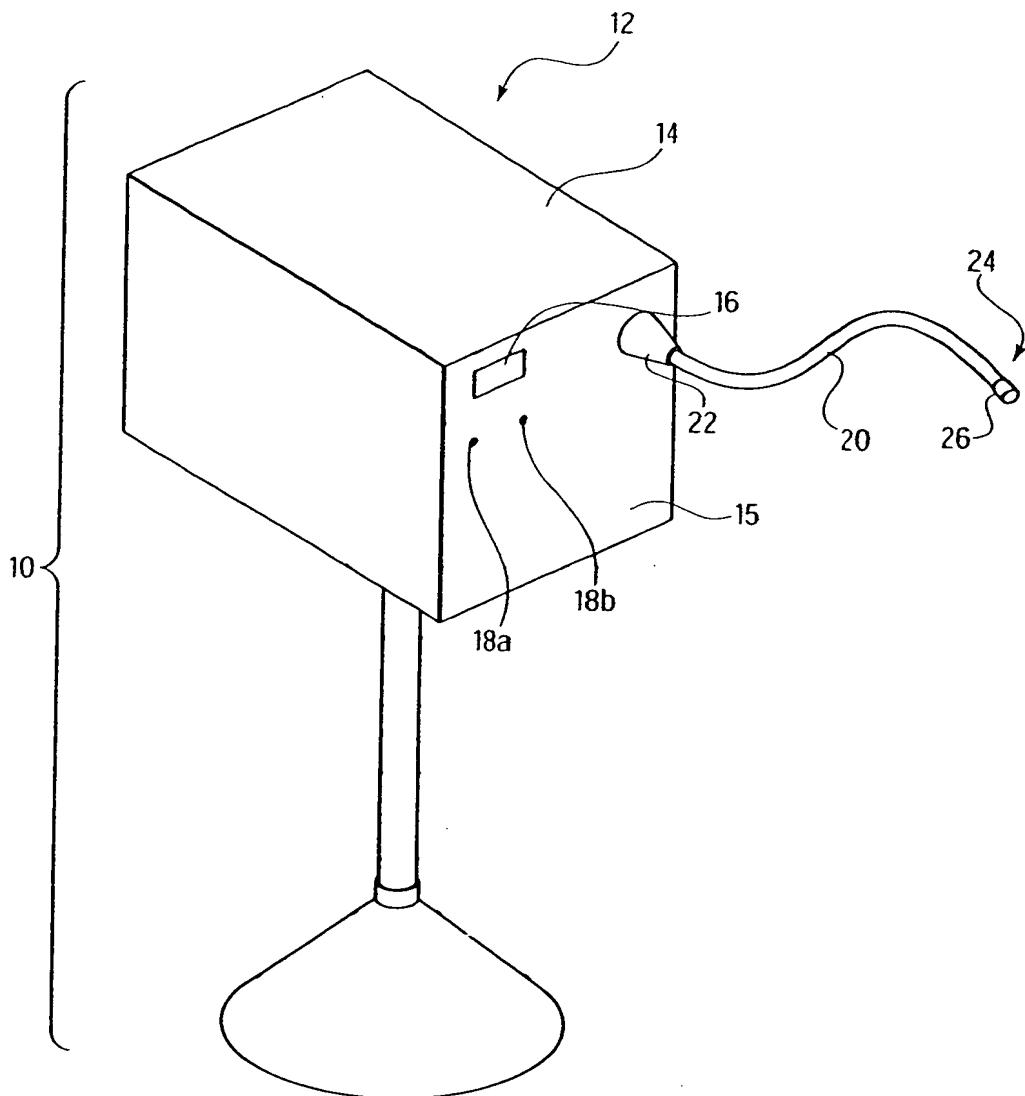
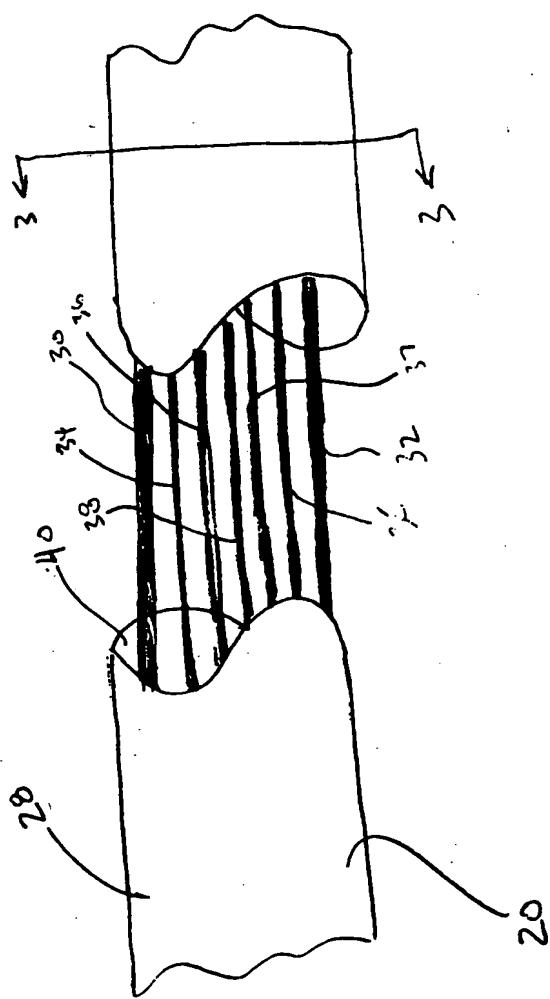
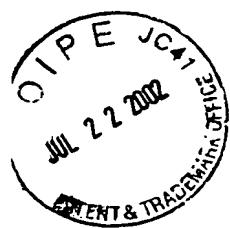


Fig. 1

FIG. 2





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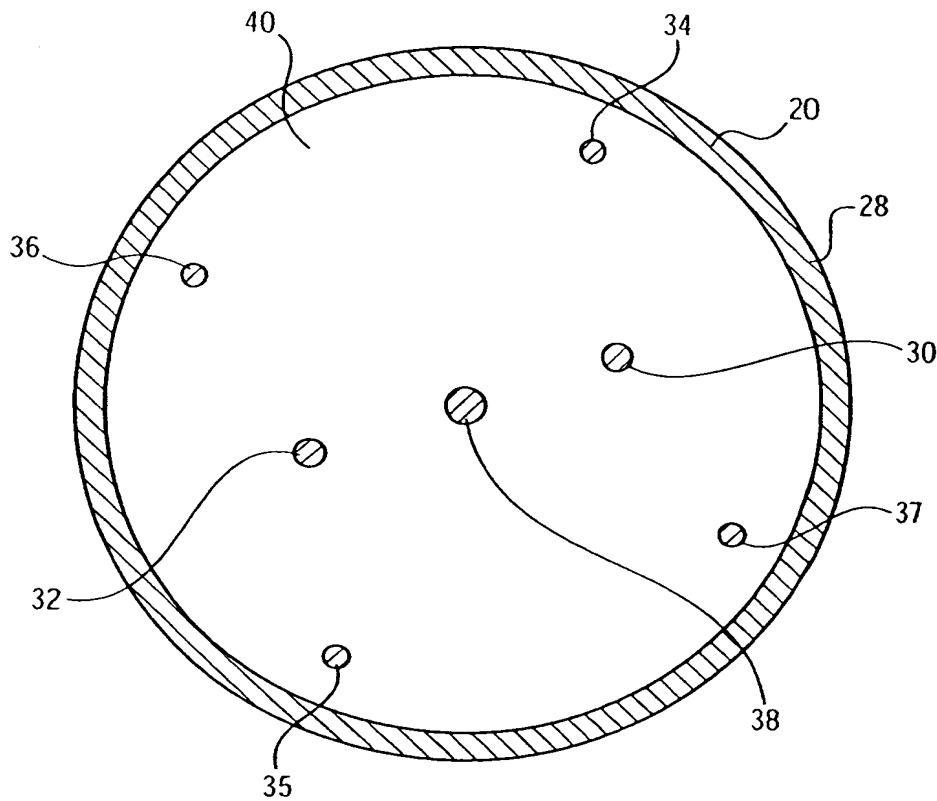


Fig. 3



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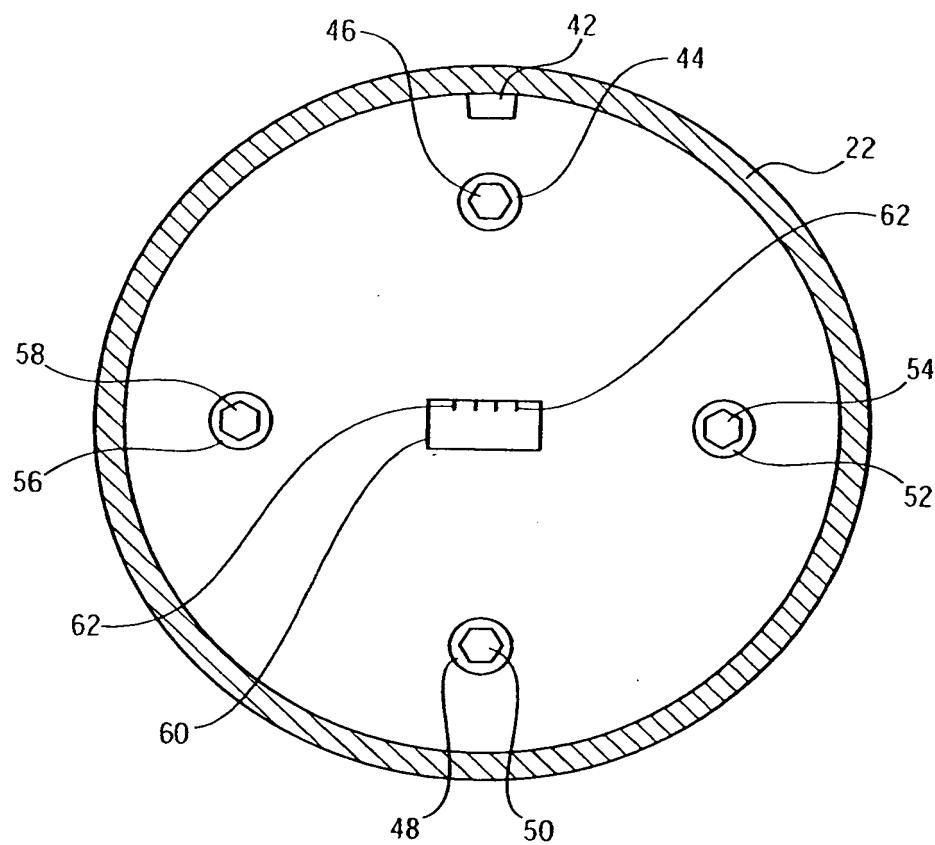


Fig. 4



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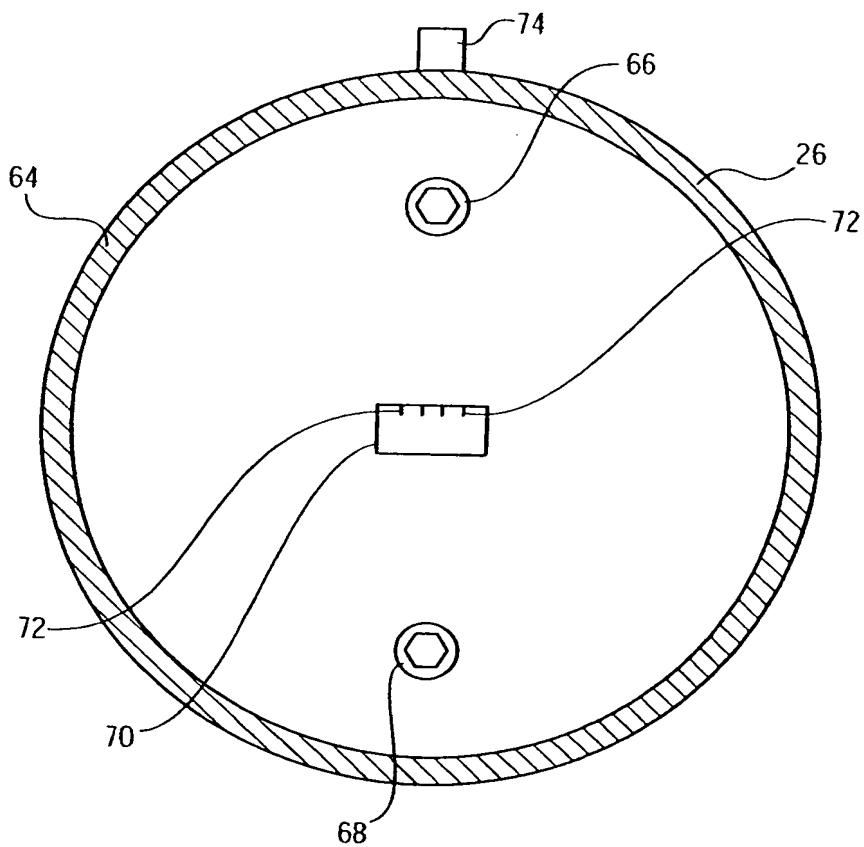


Fig. 5



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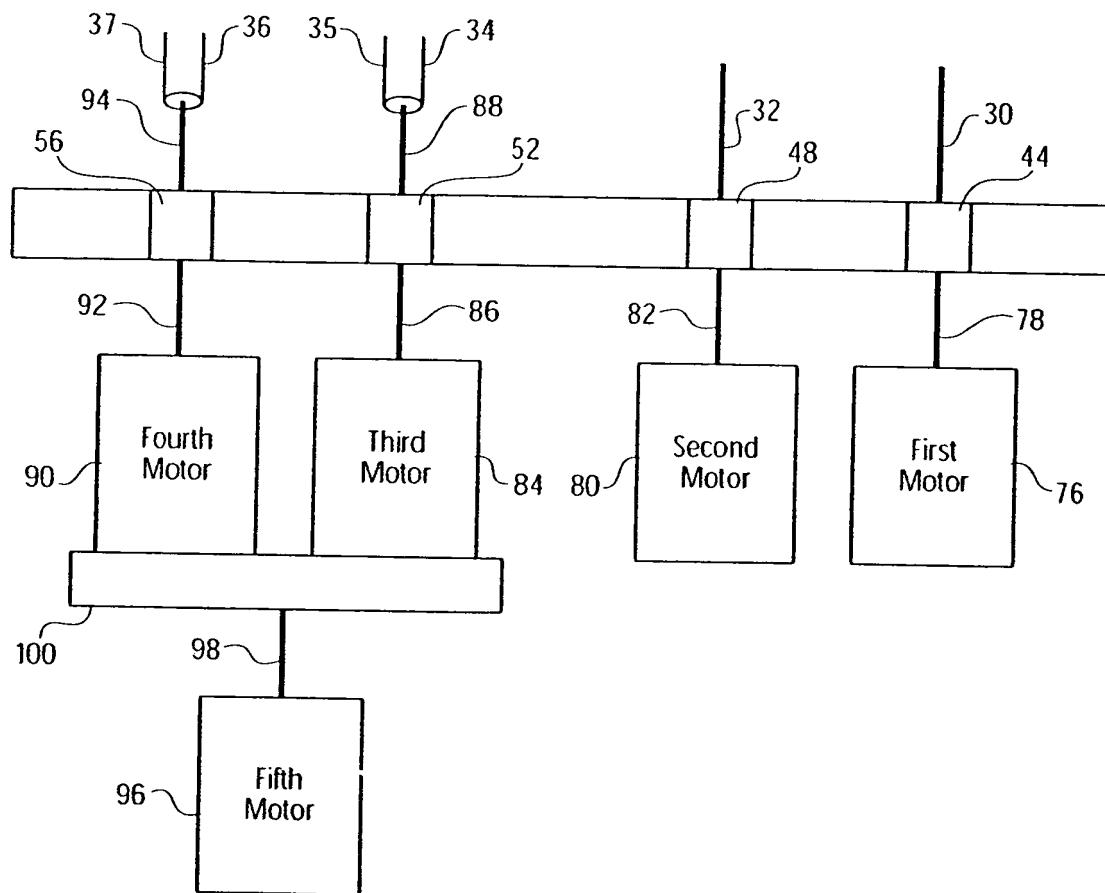
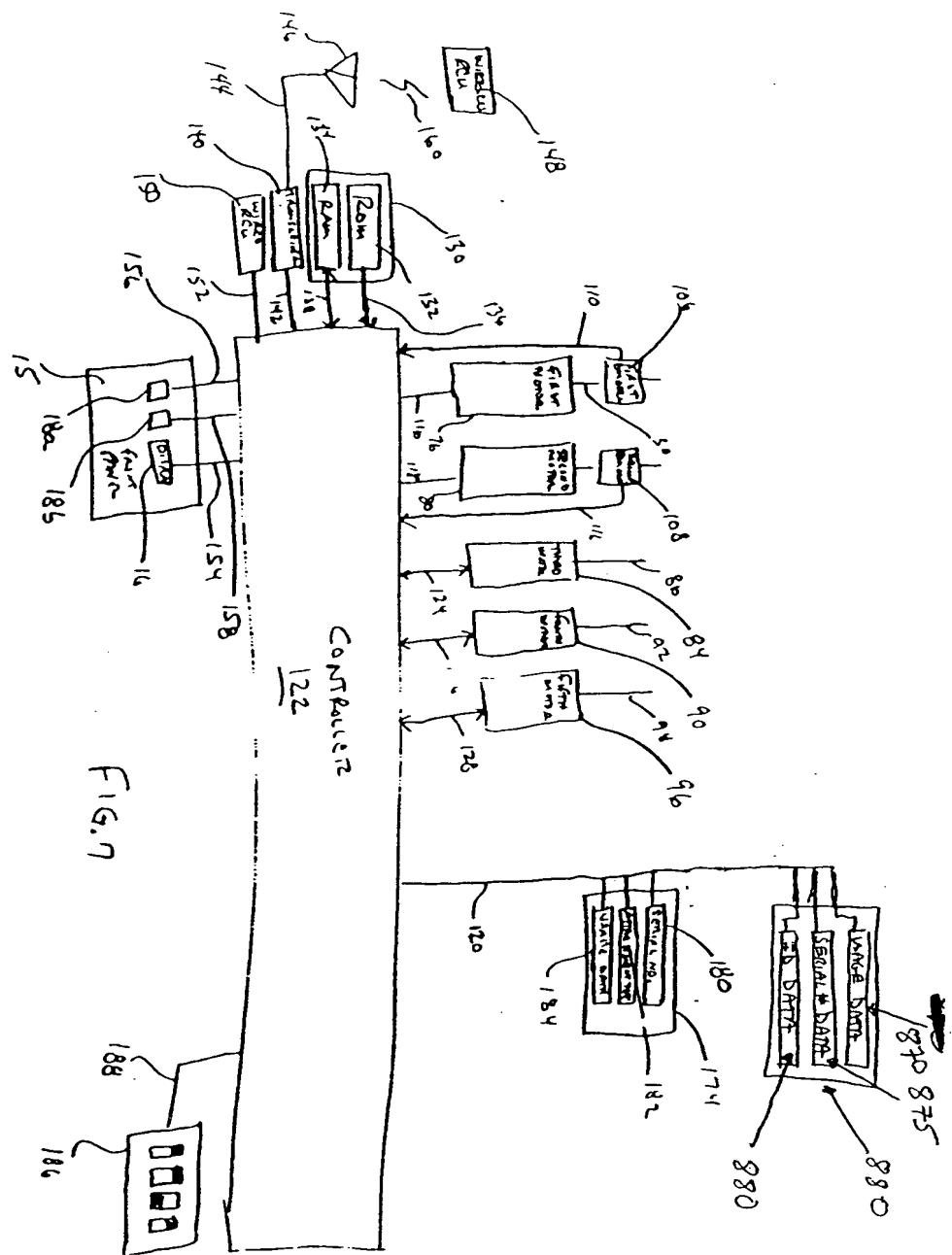


Fig.6



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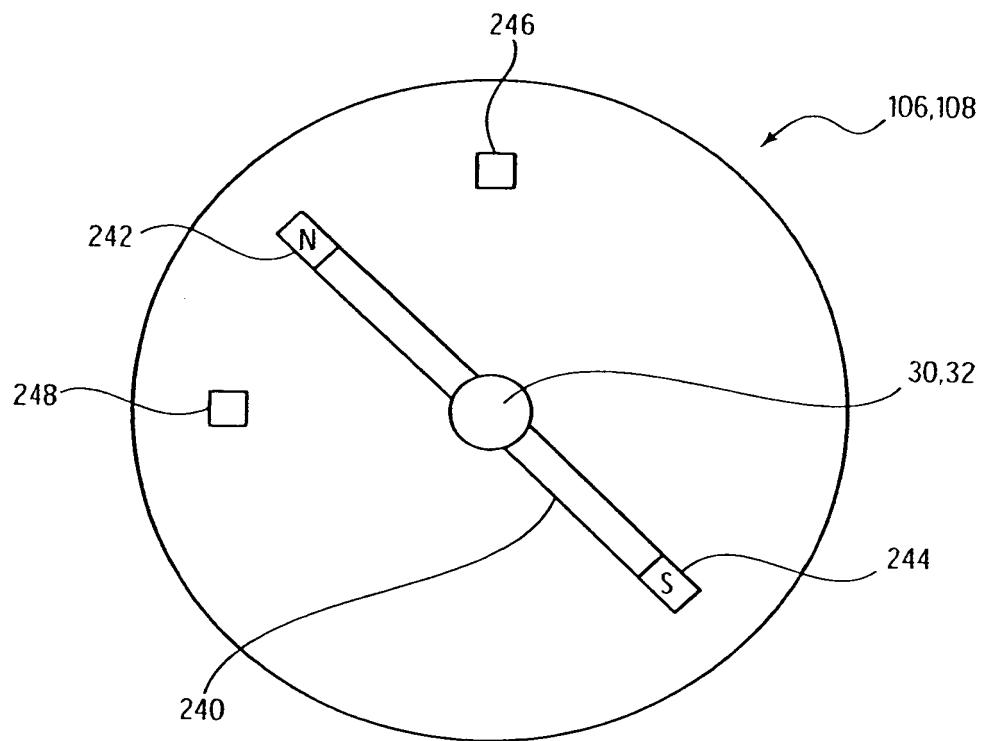


Fig. 8



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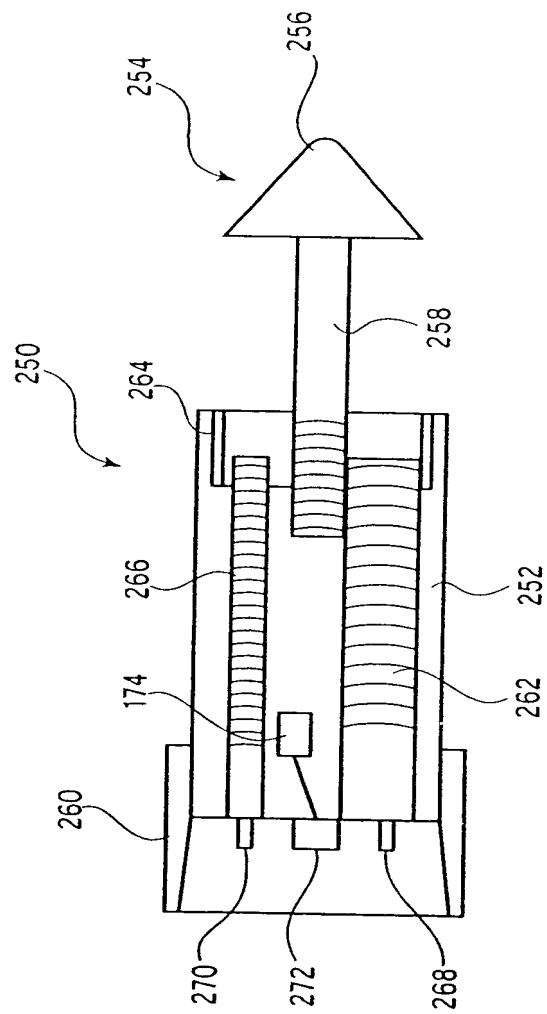


Fig. 9 ~



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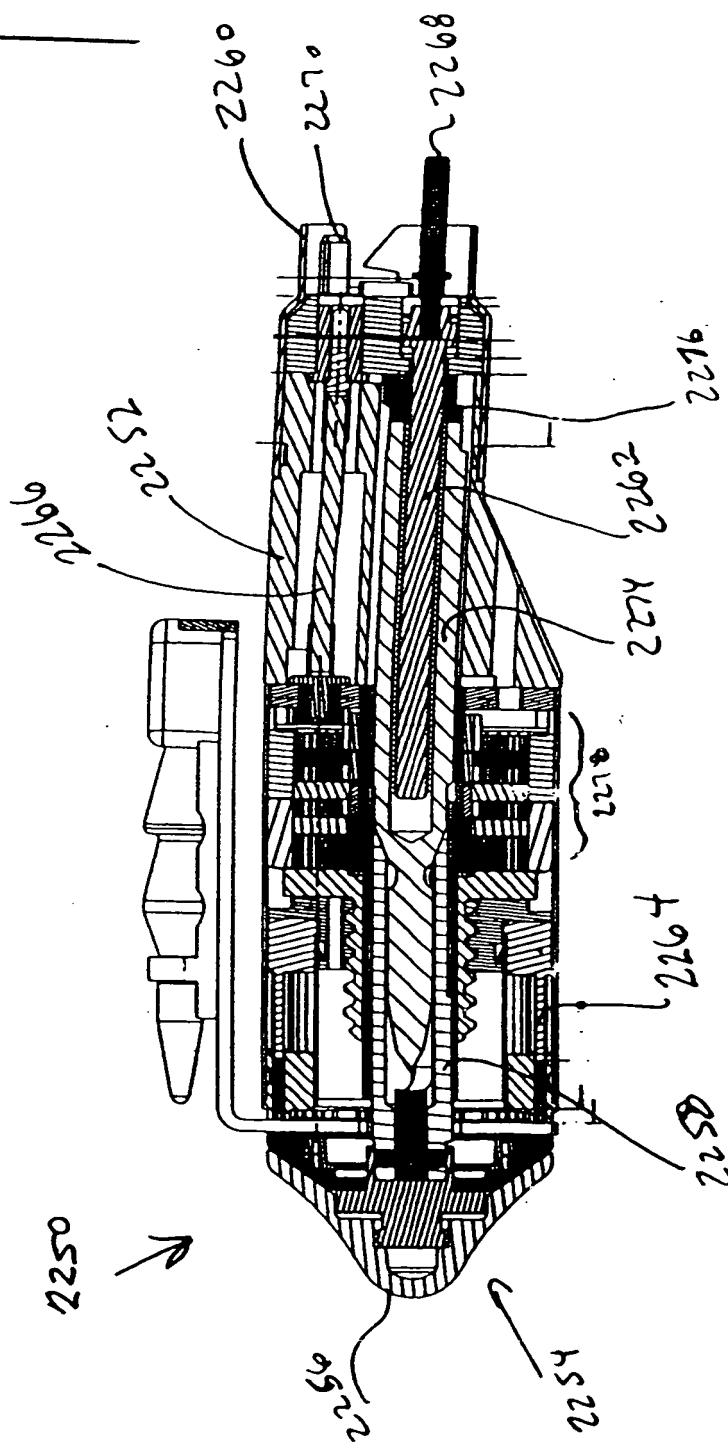


Figure 9B



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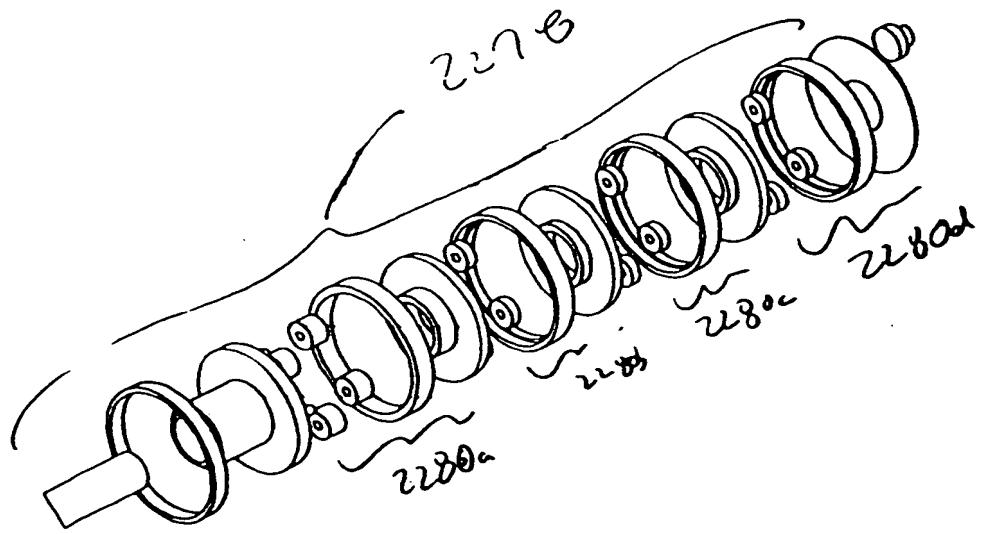


FIG. 9C



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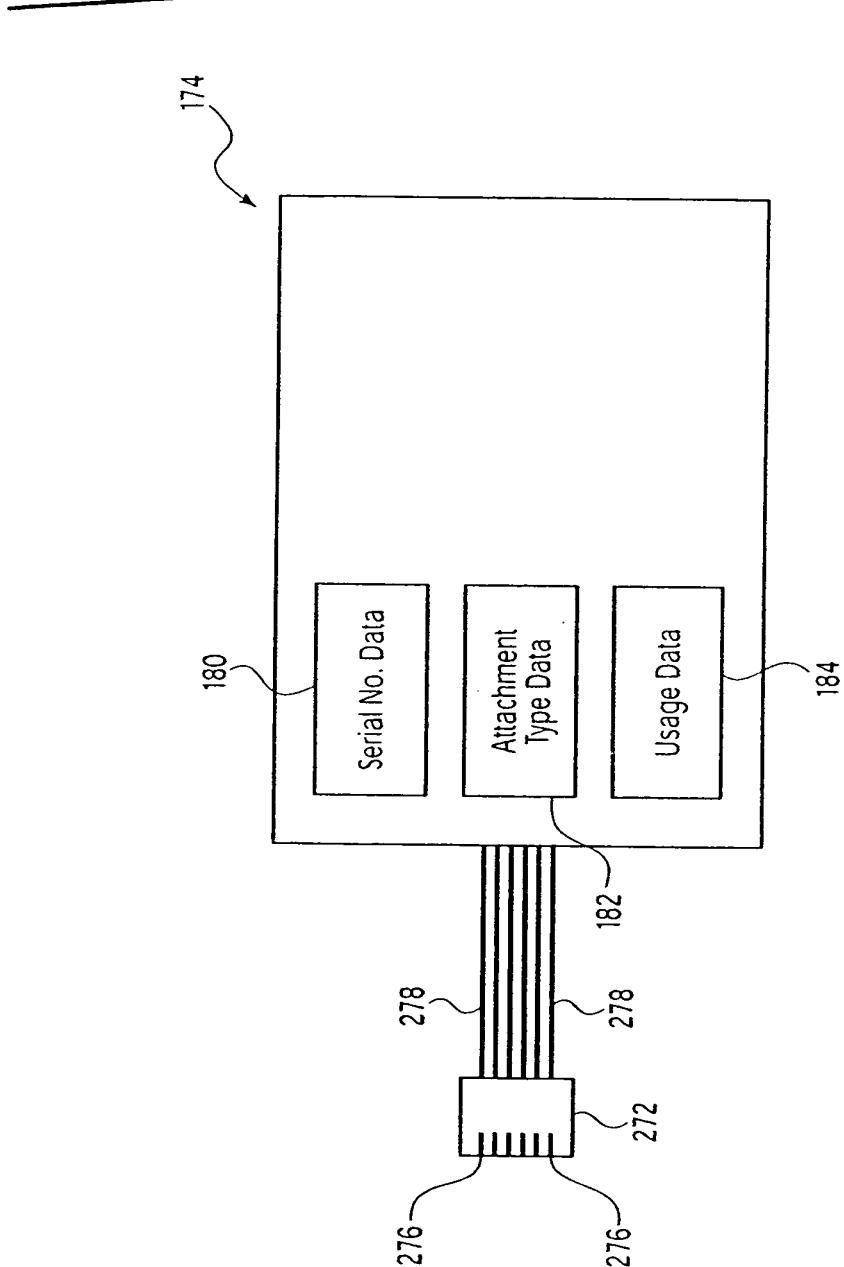


Fig. 10



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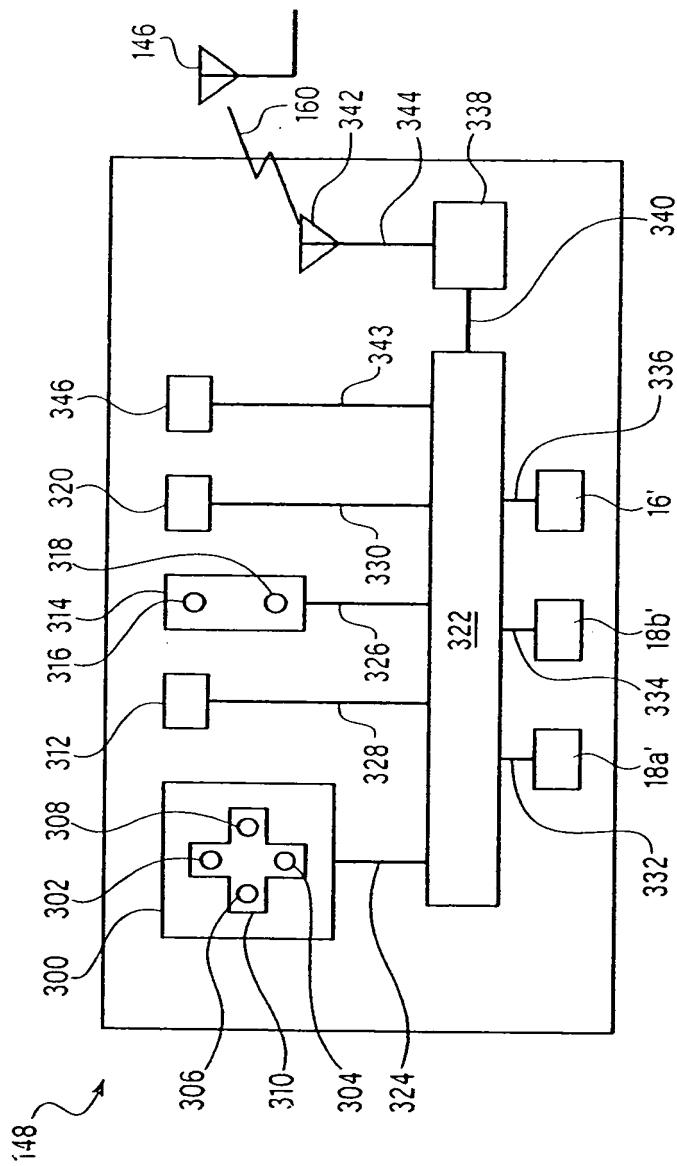


Fig. 11

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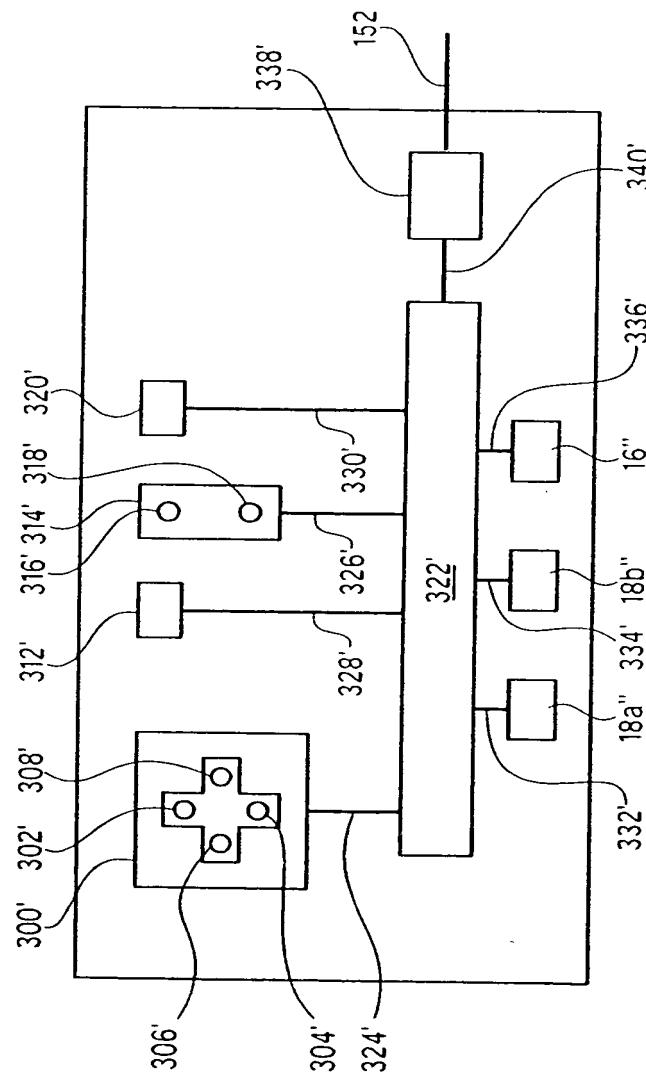
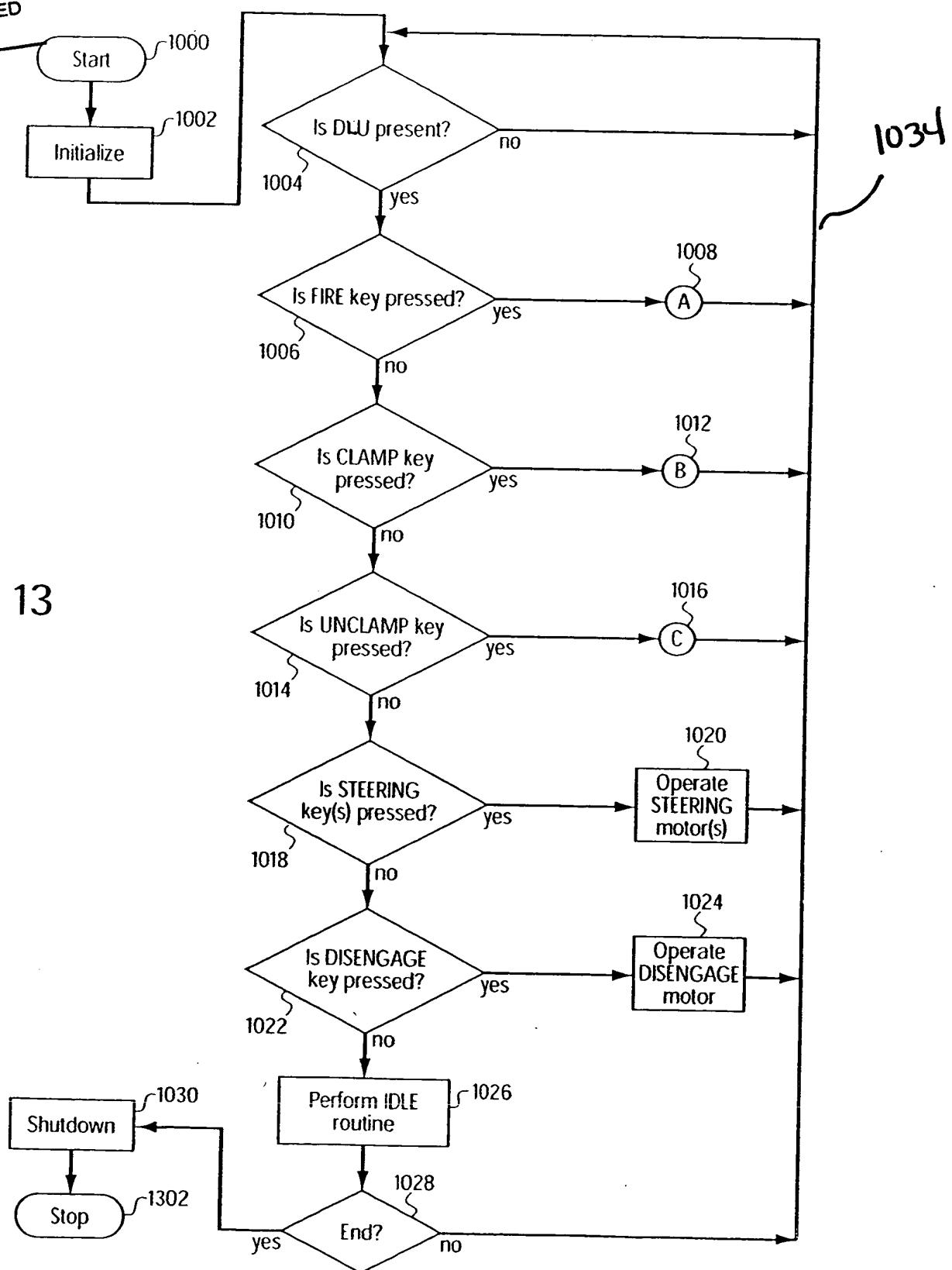


Fig. 12



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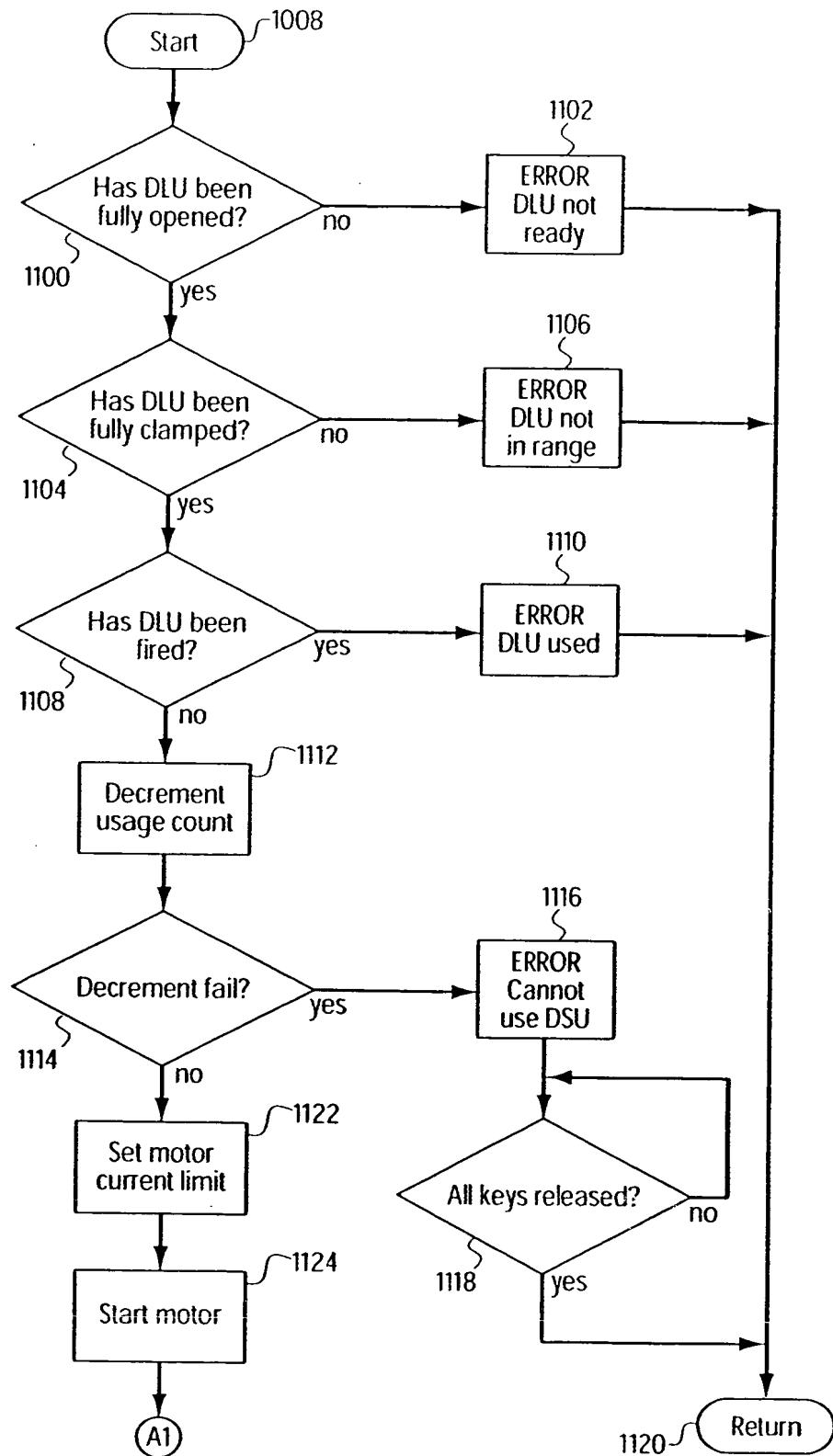
Fig. 13





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Fig. 14a





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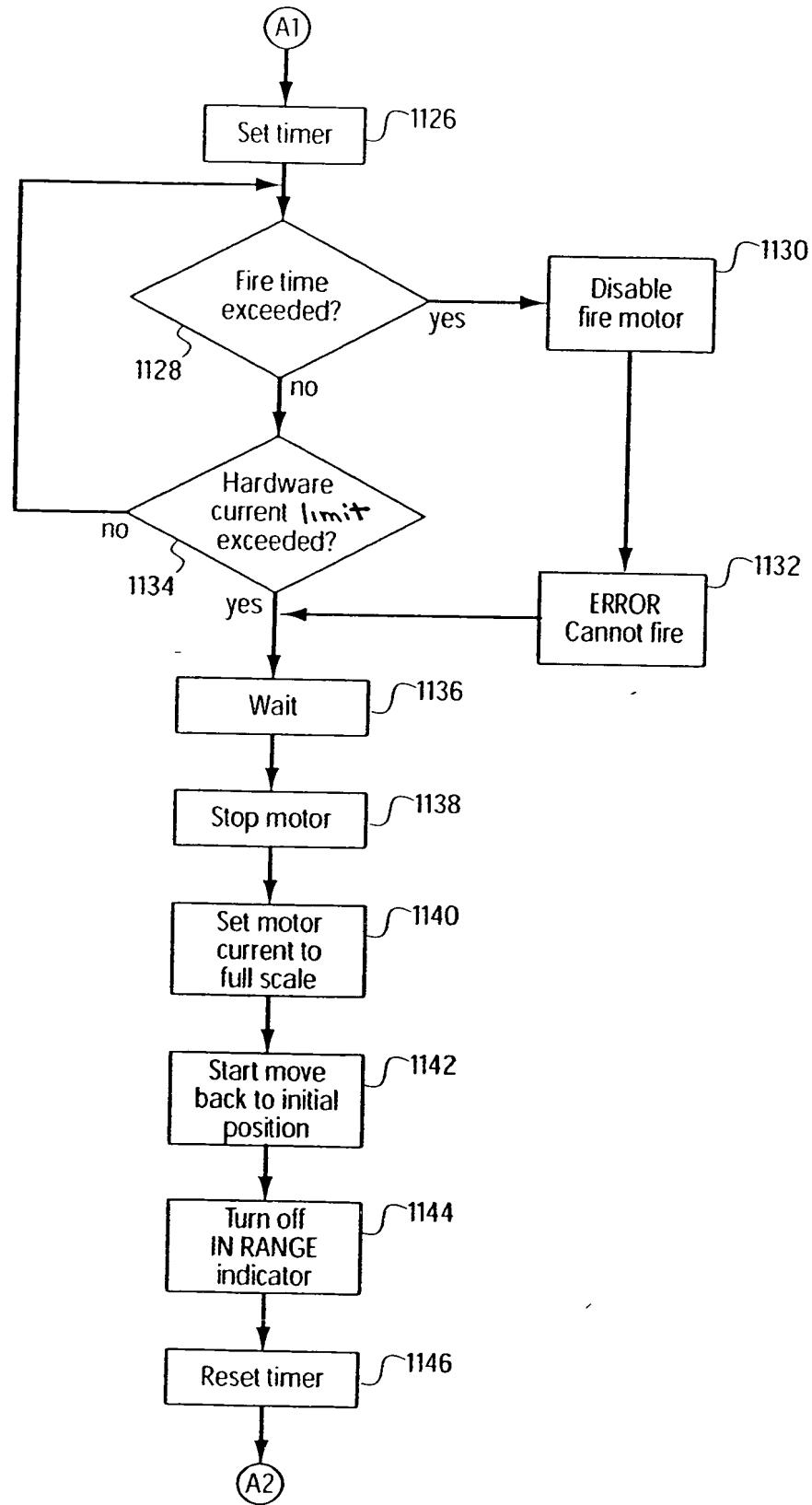
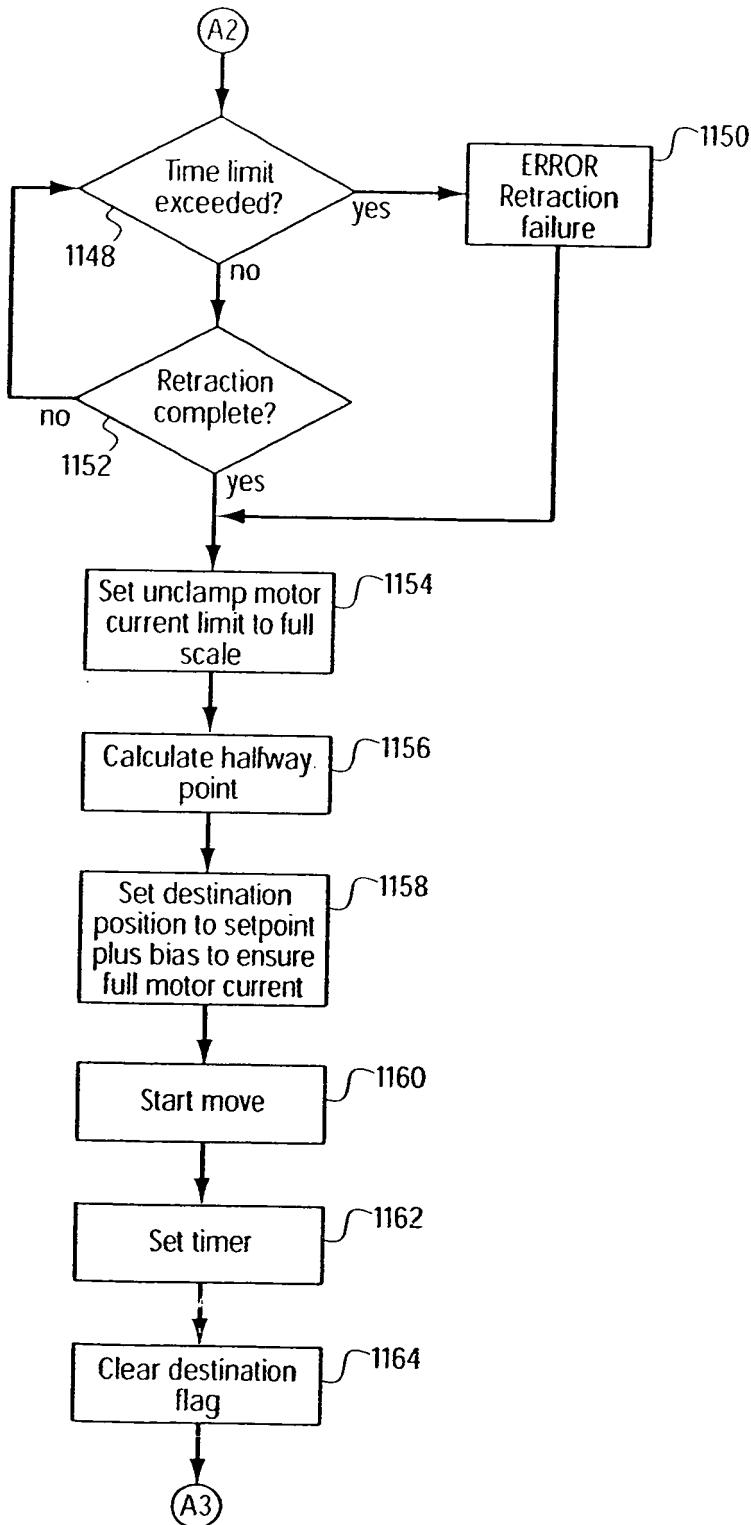


Fig. 14b



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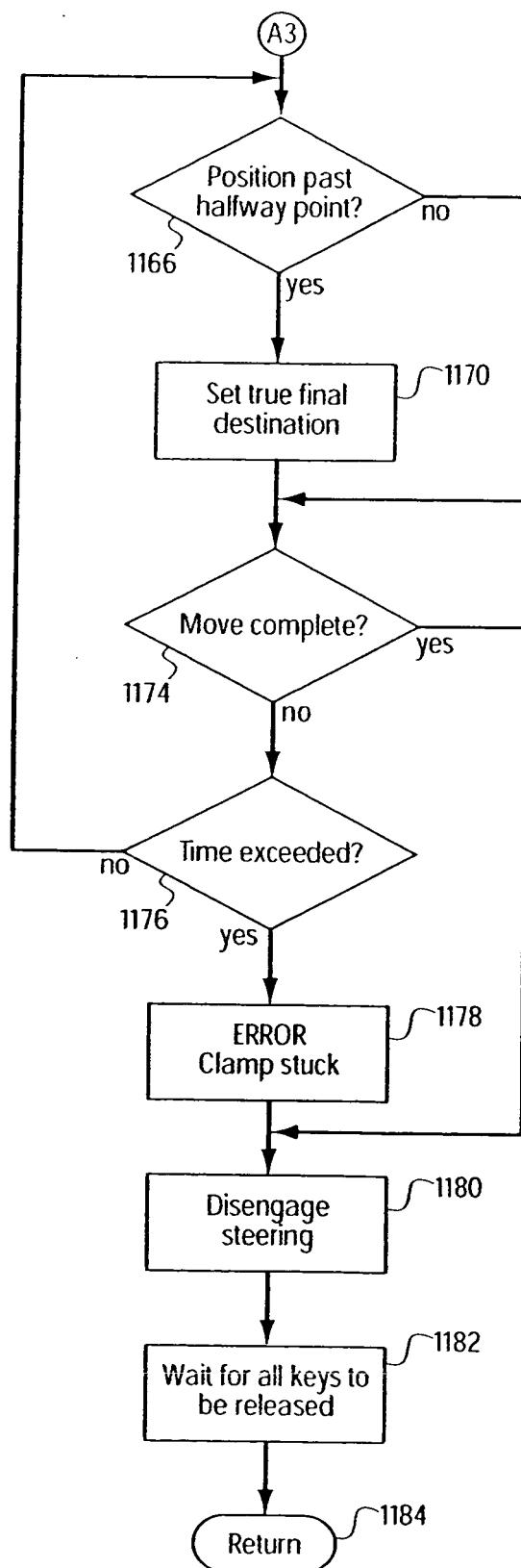
Fig. 14c





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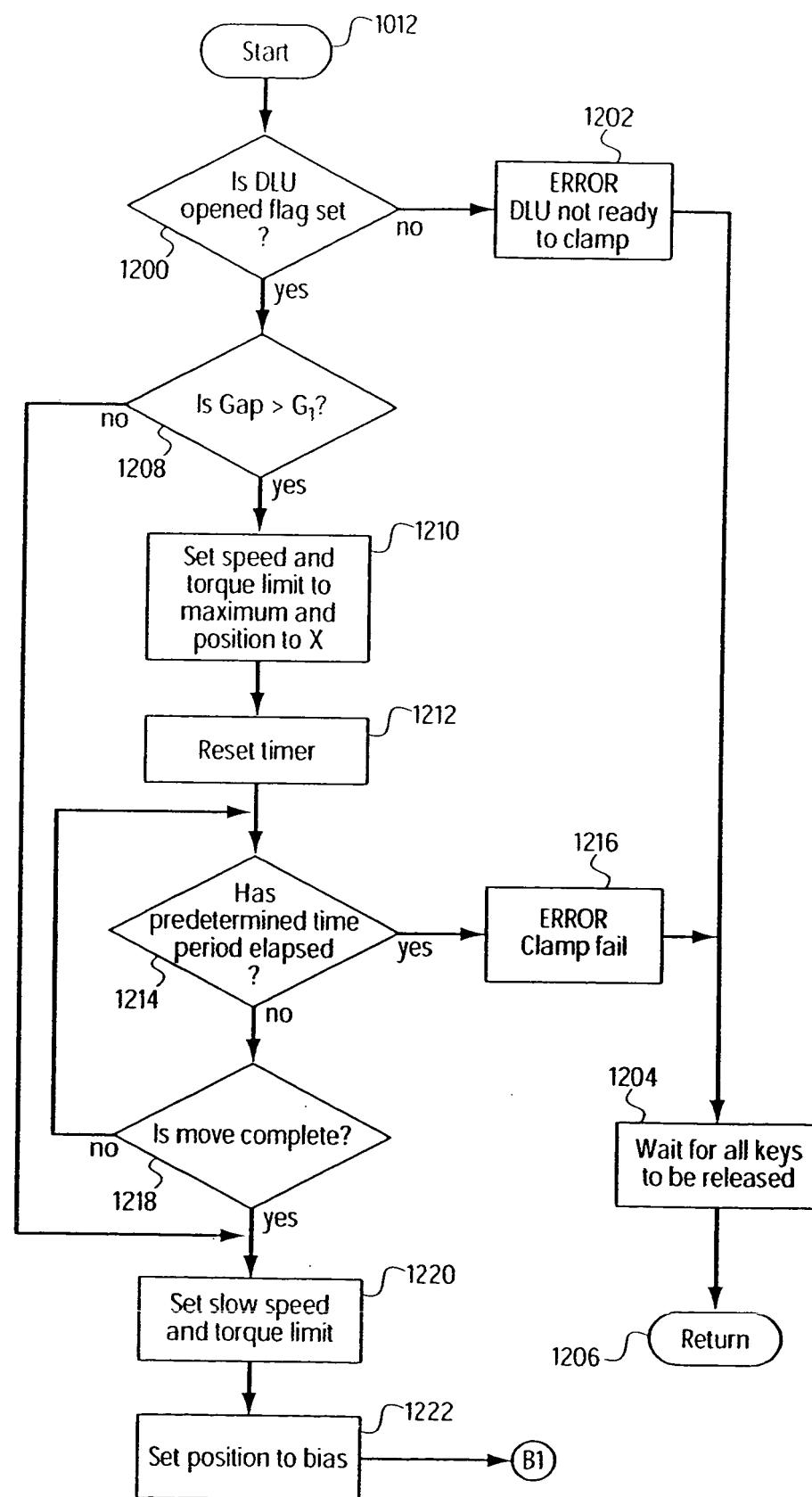
Fig. 14d





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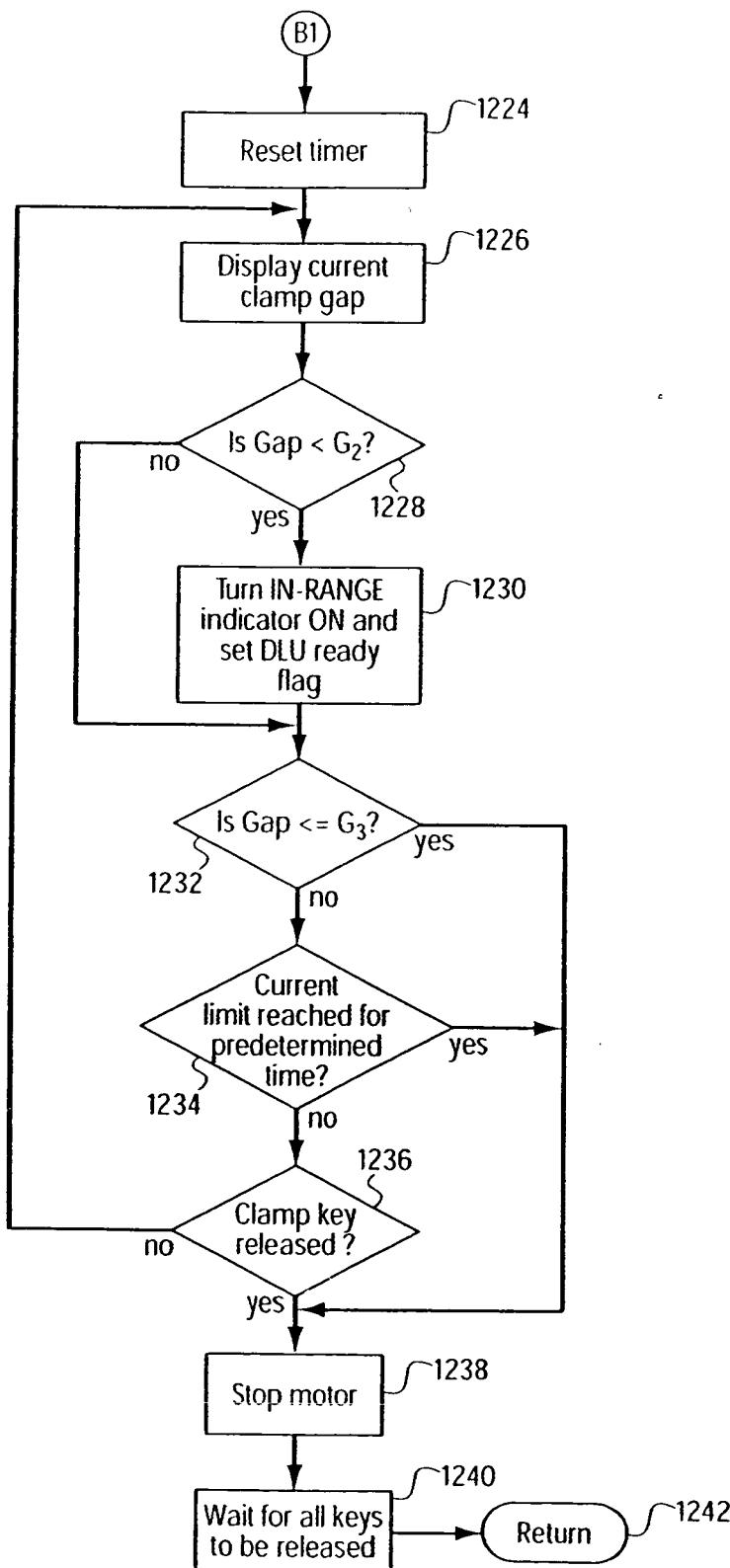
Fig.15a





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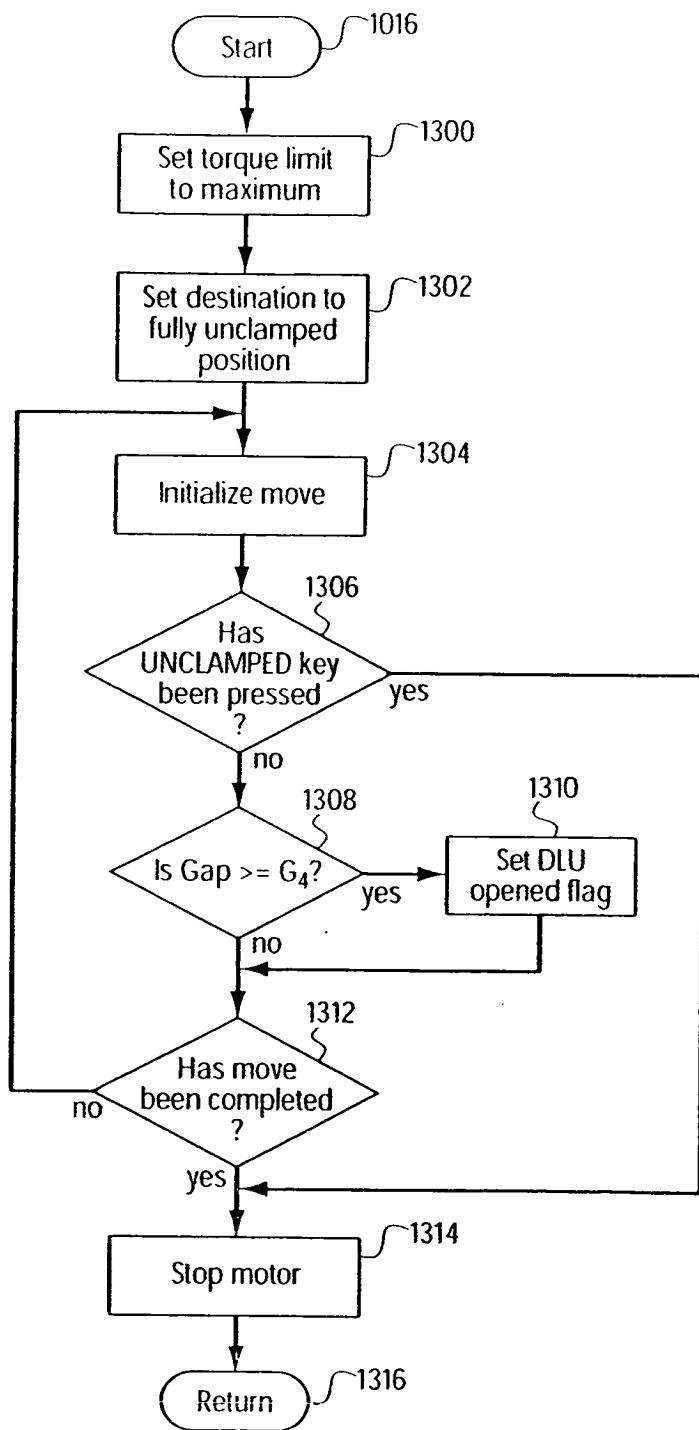
Fig.15b





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Fig.16





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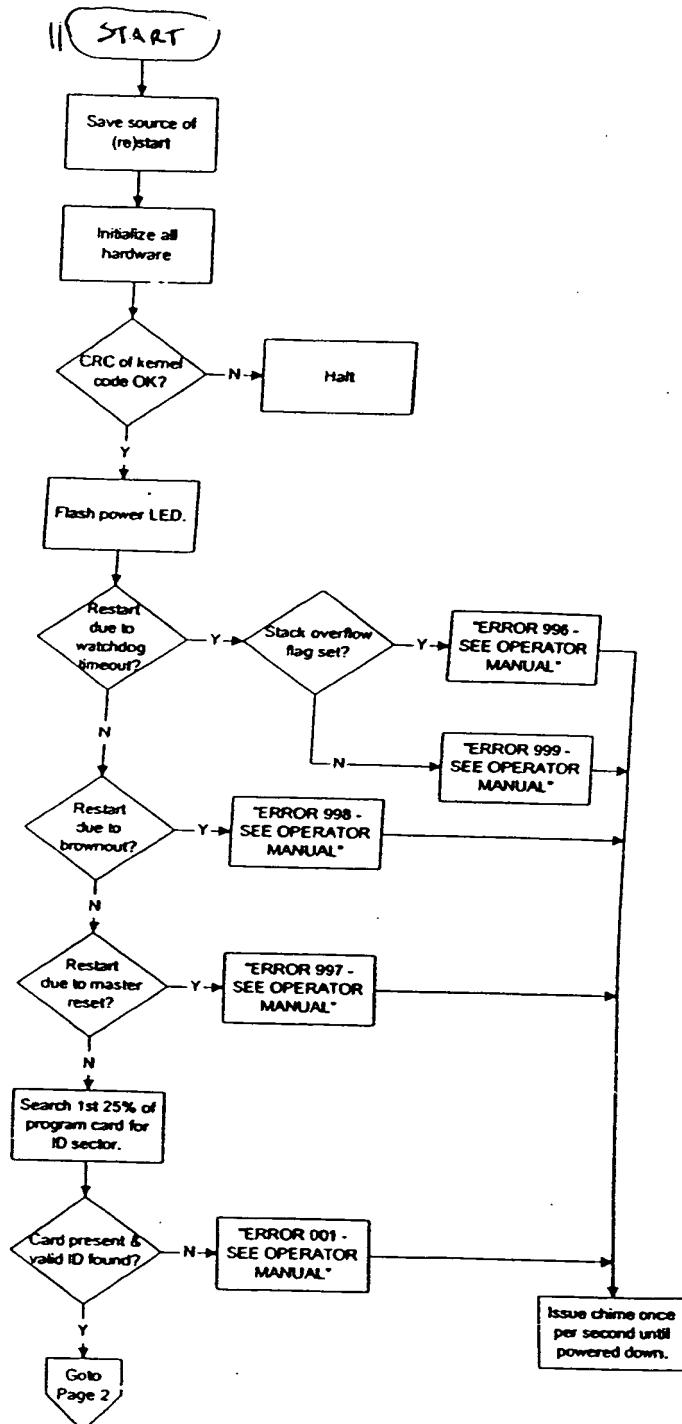


FIG. 17a



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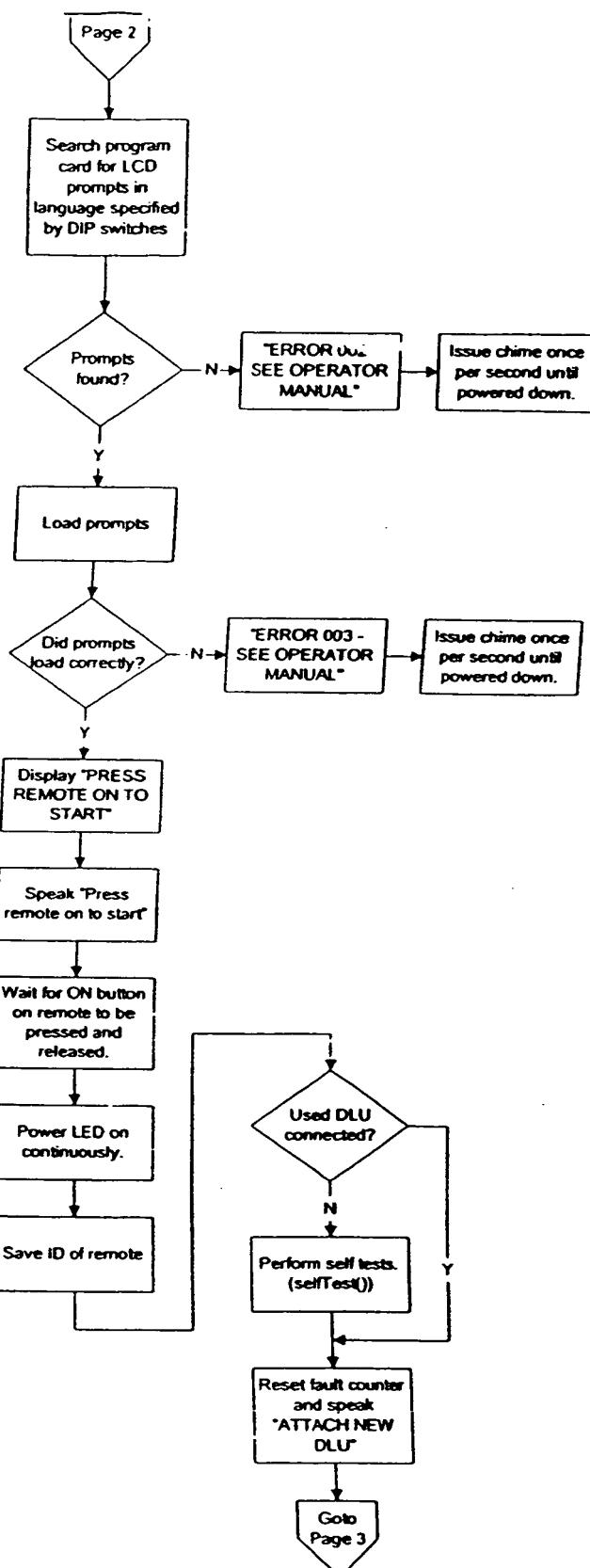


FIG. 17b



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Main processing loop

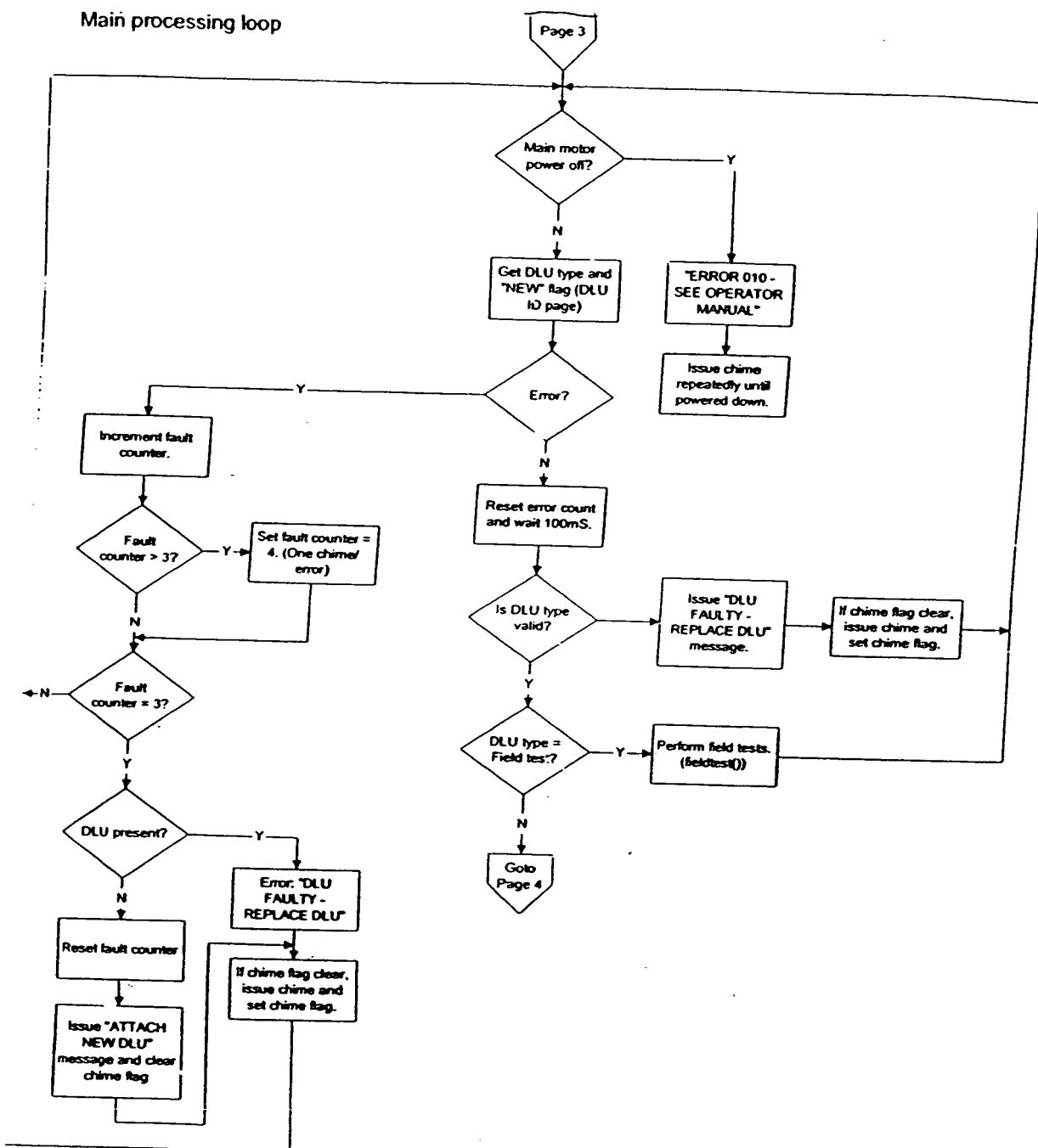


FIG. 19c

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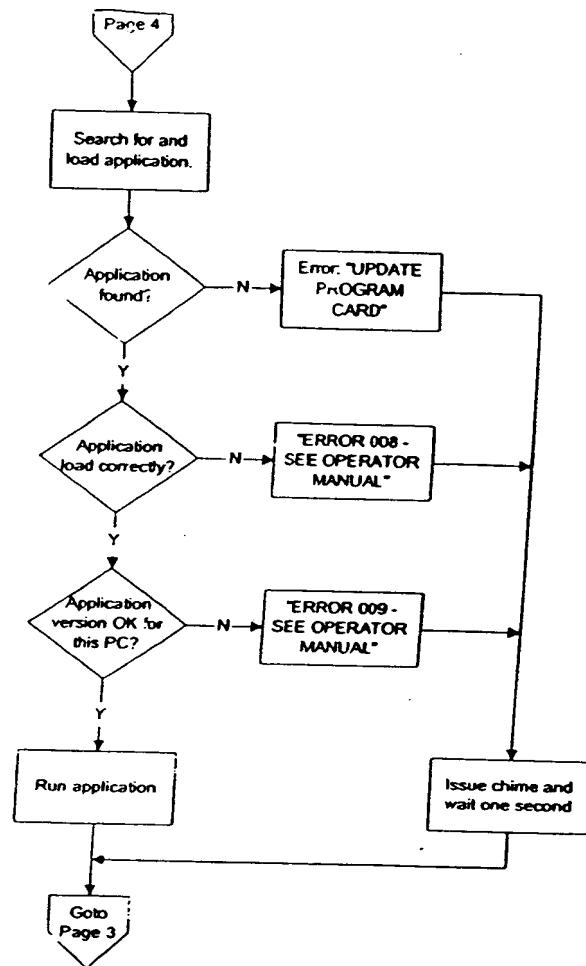


FIG. 17d



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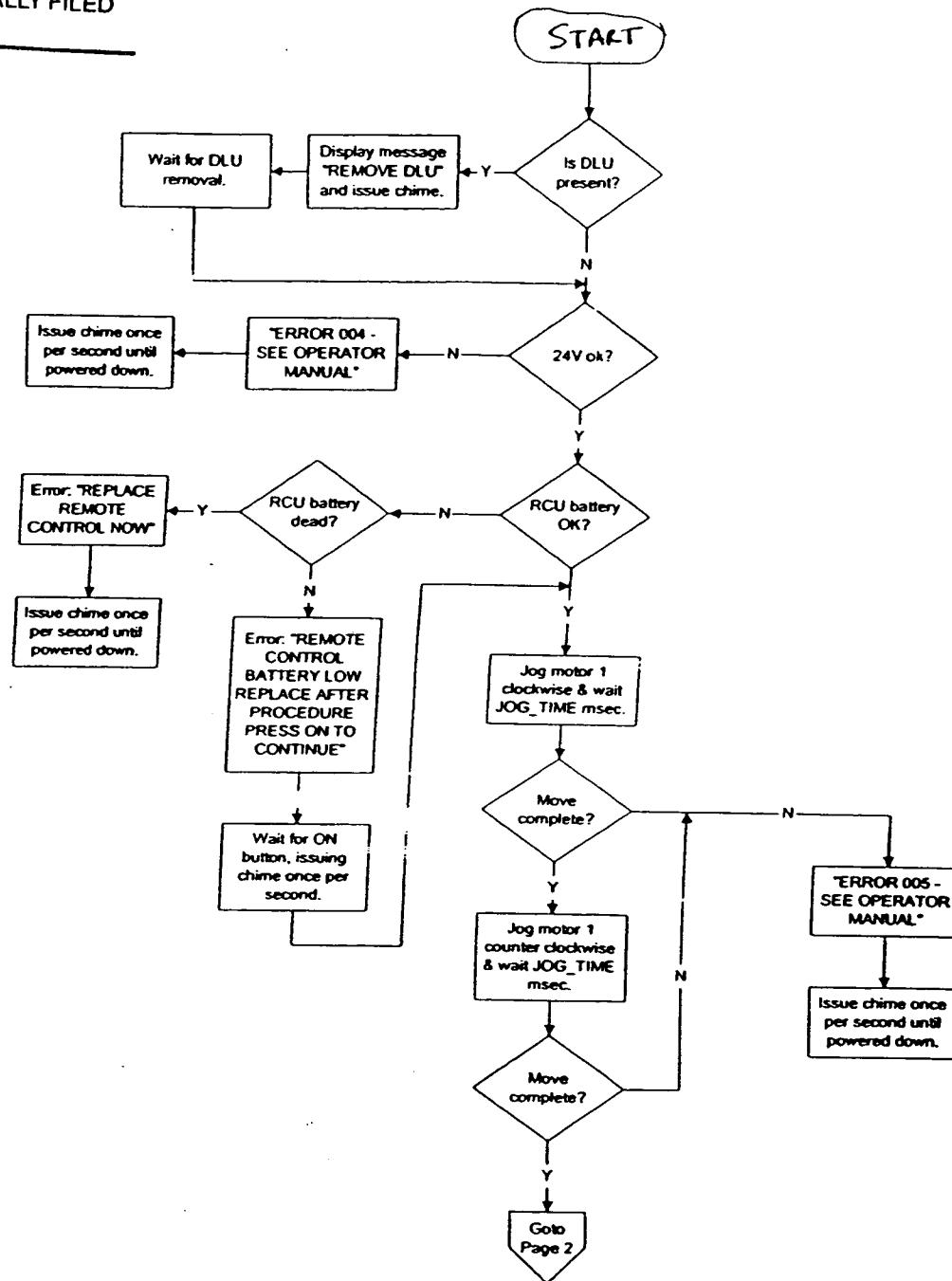


FIG. 18a



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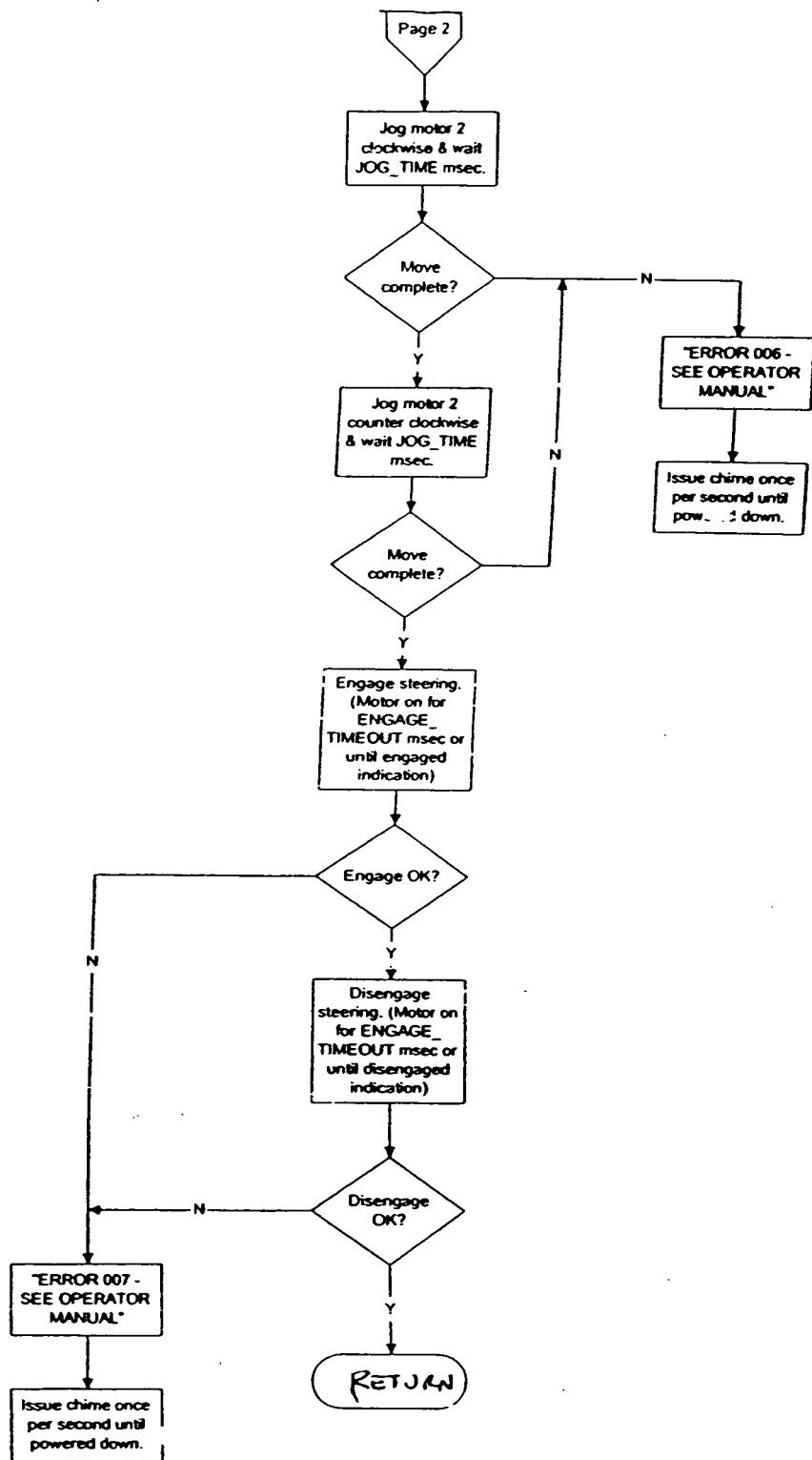


FIG. 18b



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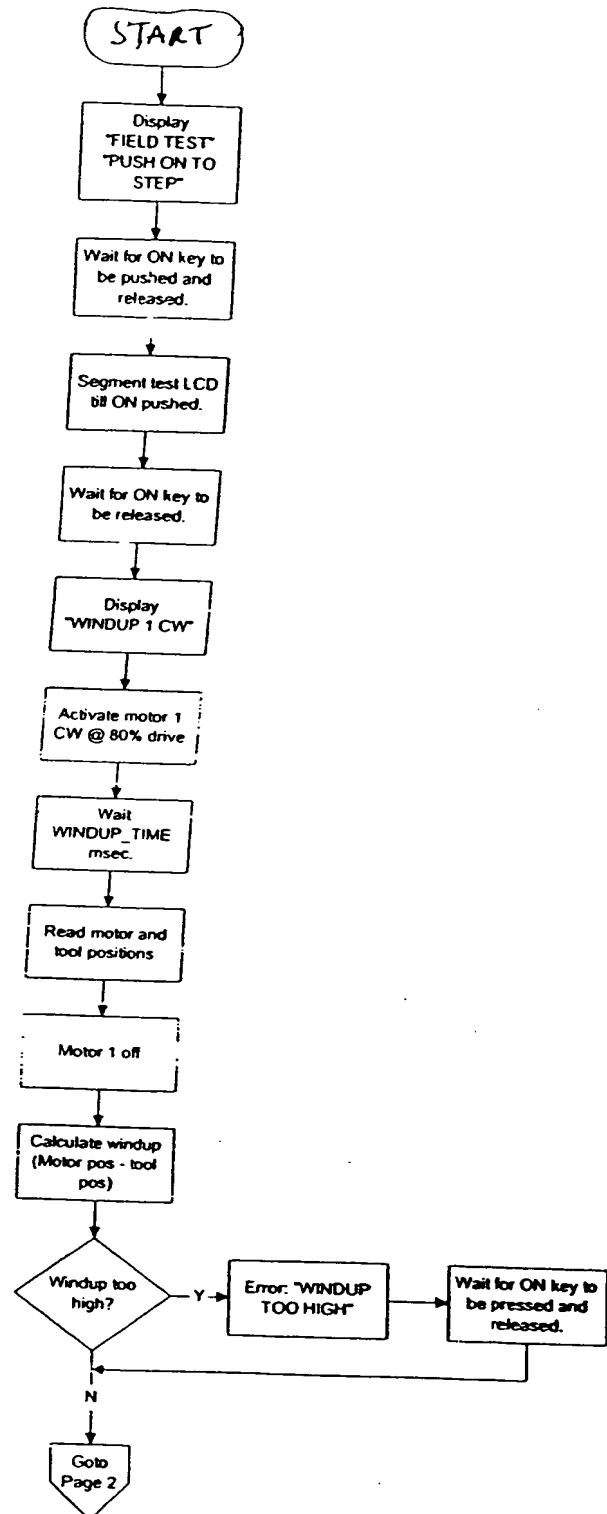


FIG. 19a



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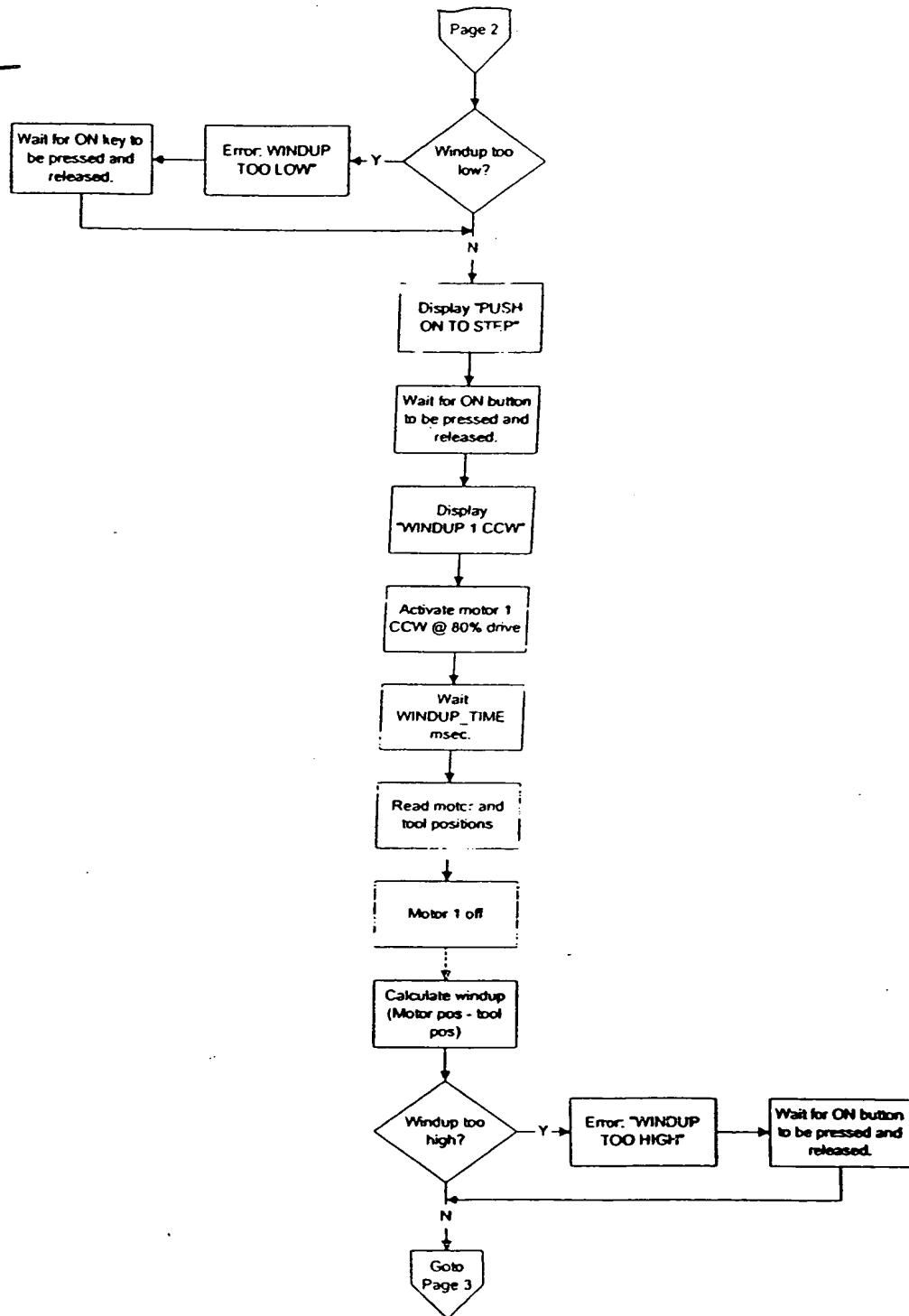


FIG. 19b

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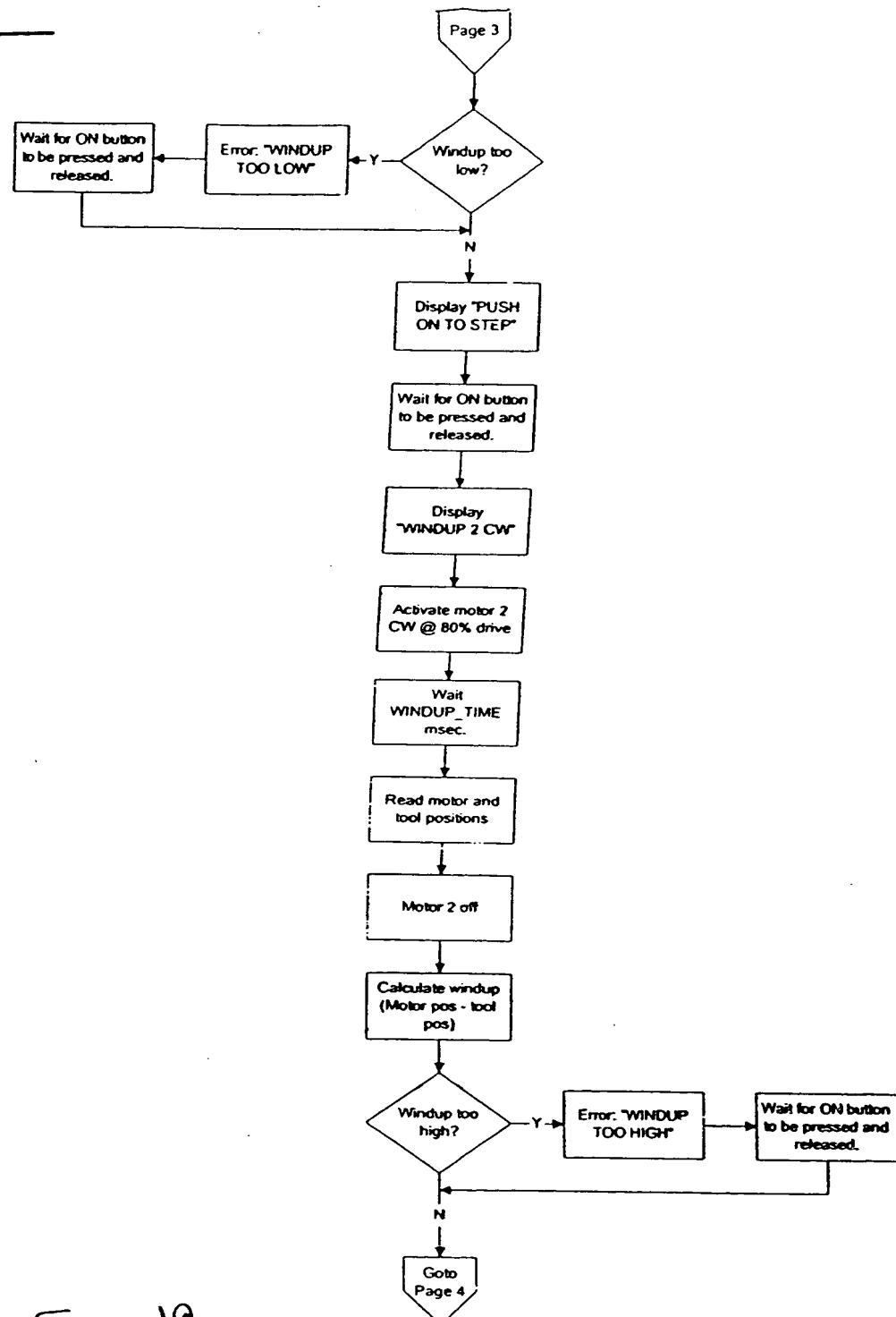
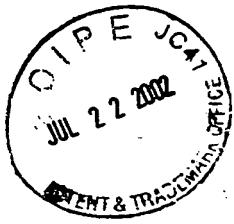


FIG. 19c



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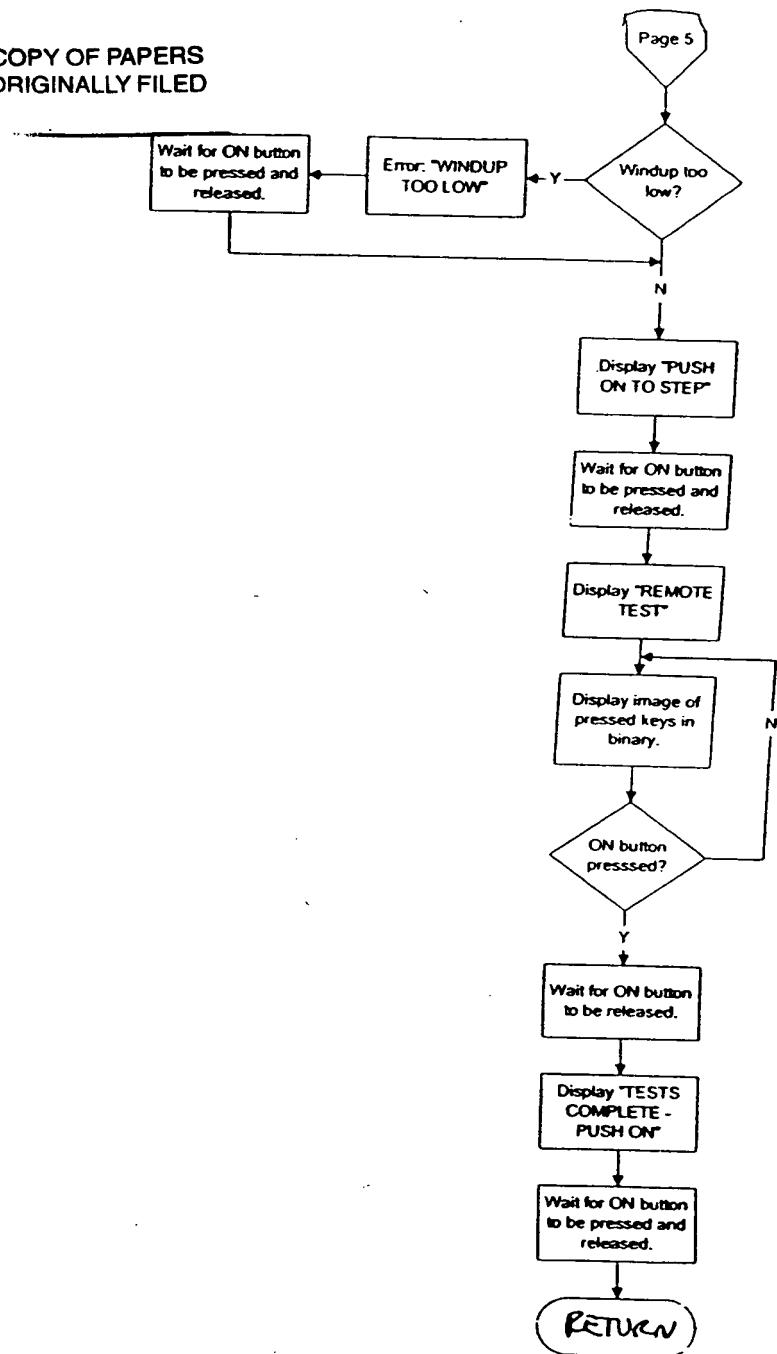


FIG. 19e



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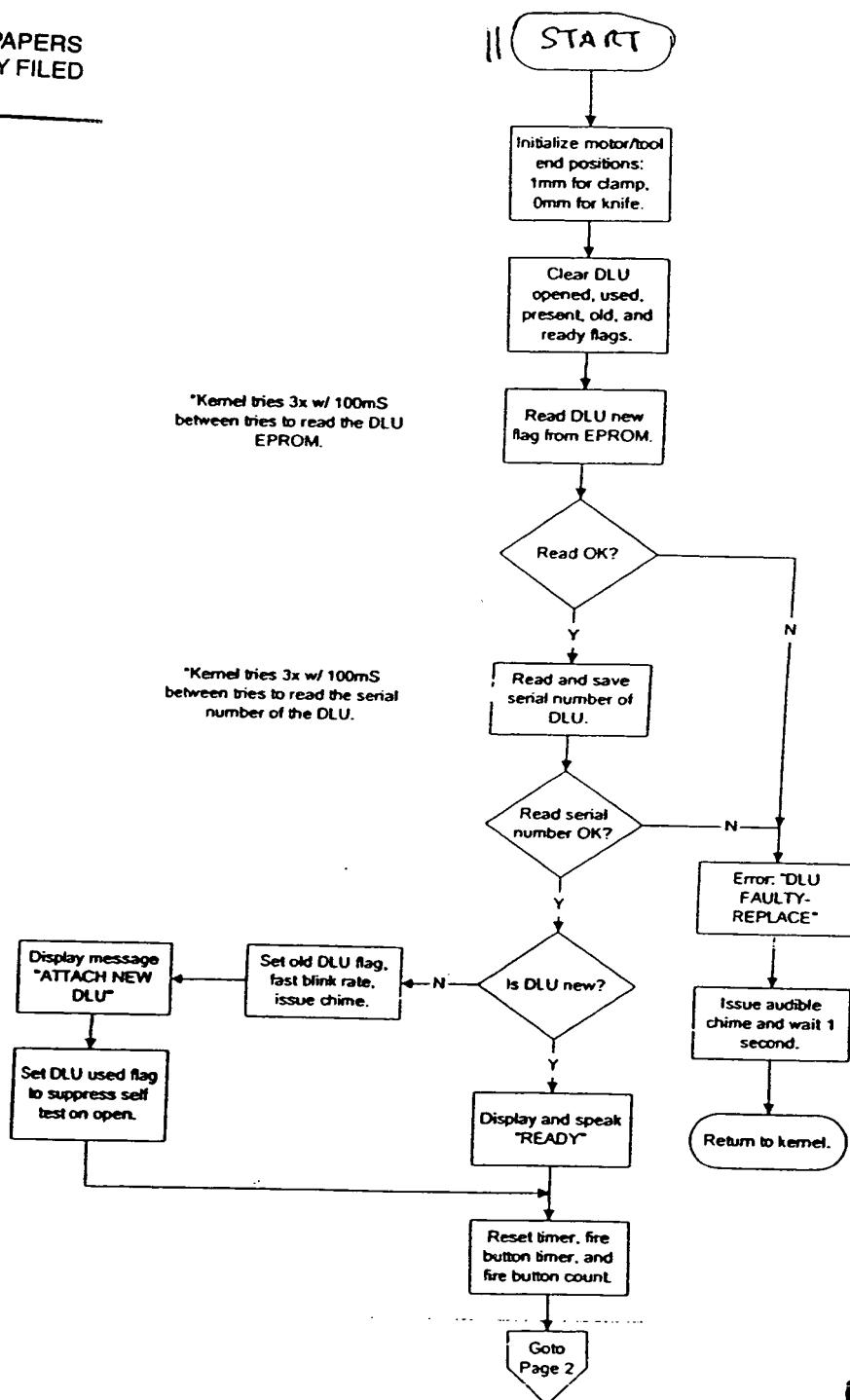


FIG. 20a



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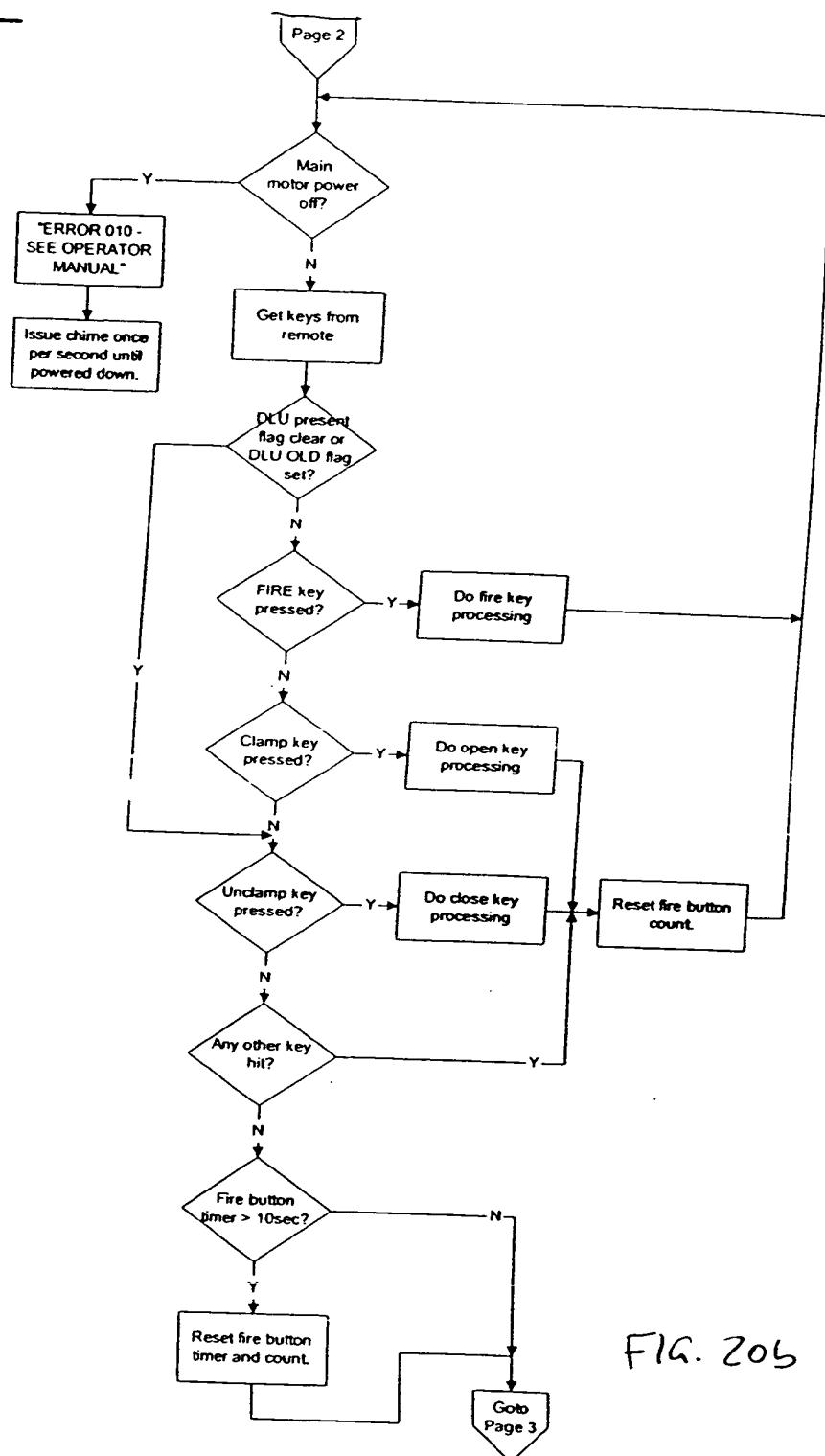
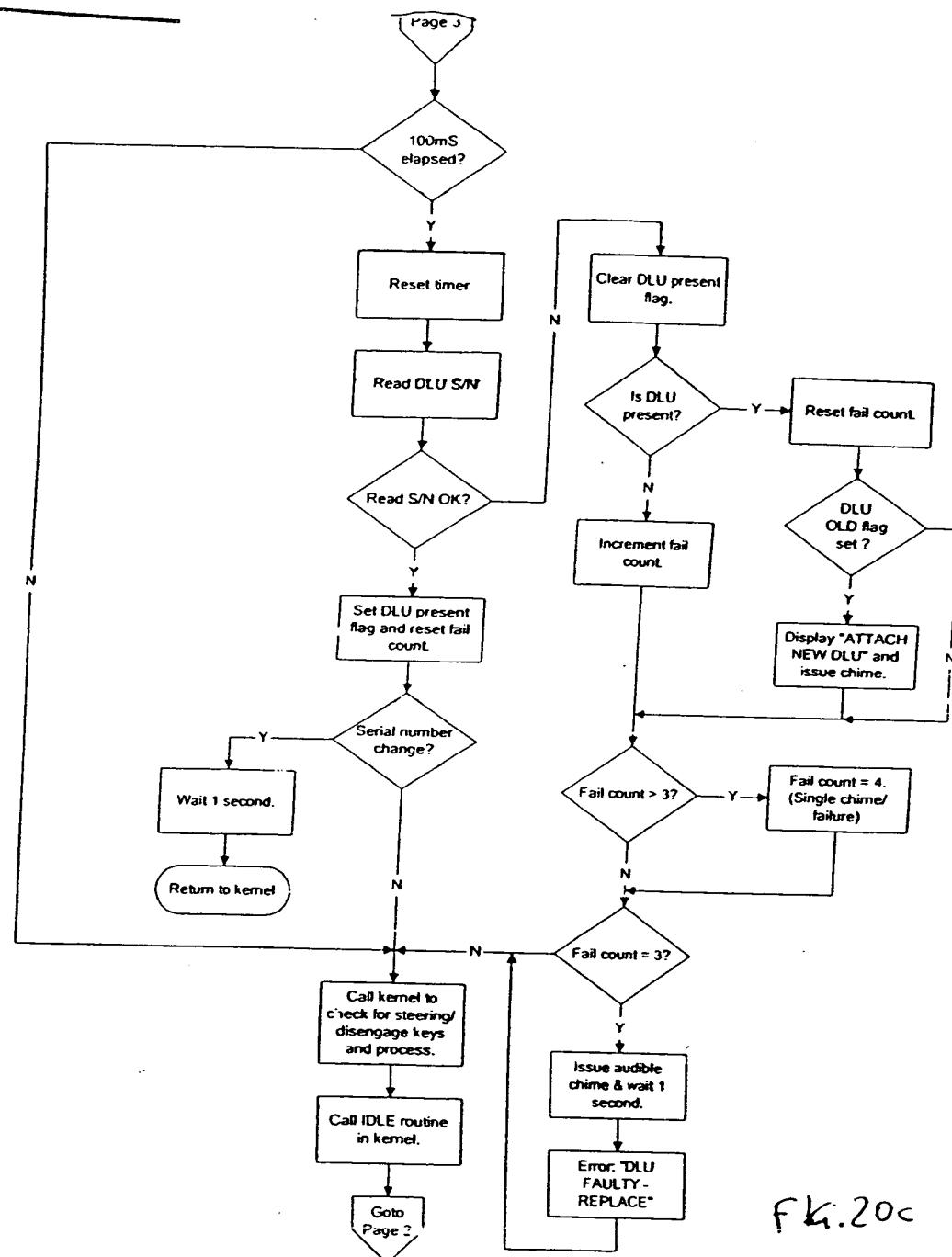


FIG. 205



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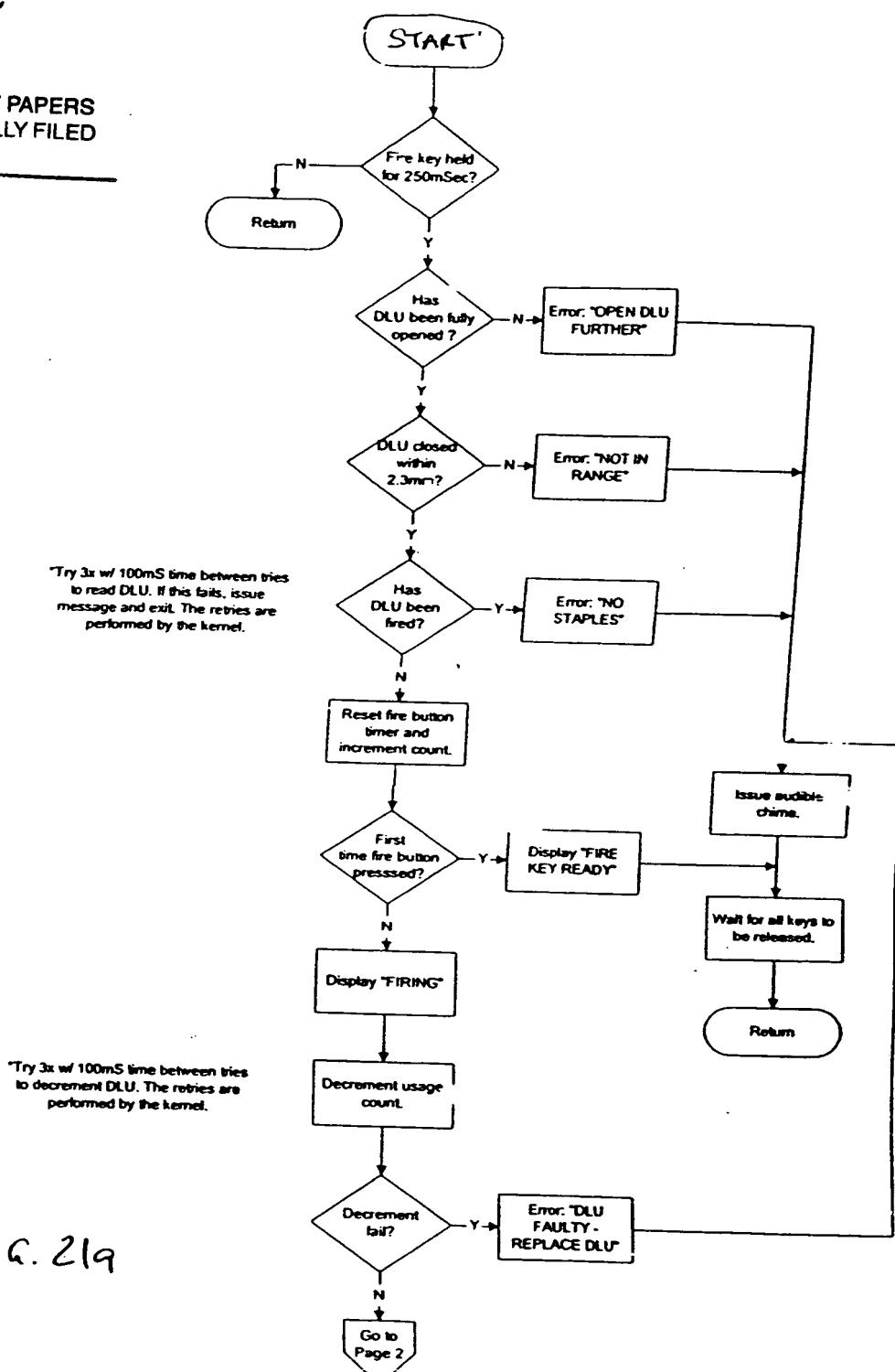


FIG. 219



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Windup threshold is
defined as
SHAFT_WINDUP_MAX

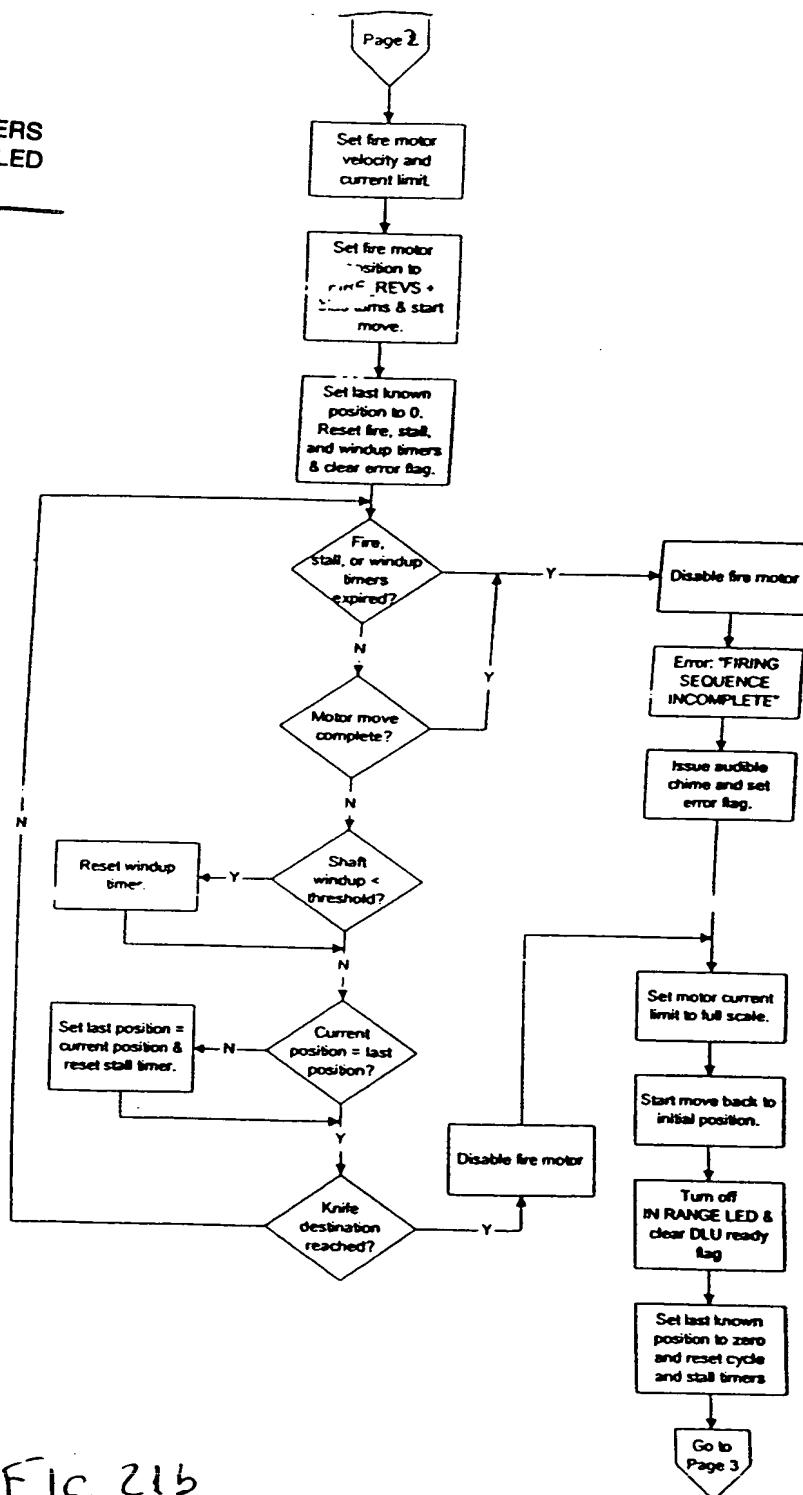


FIG. 21b

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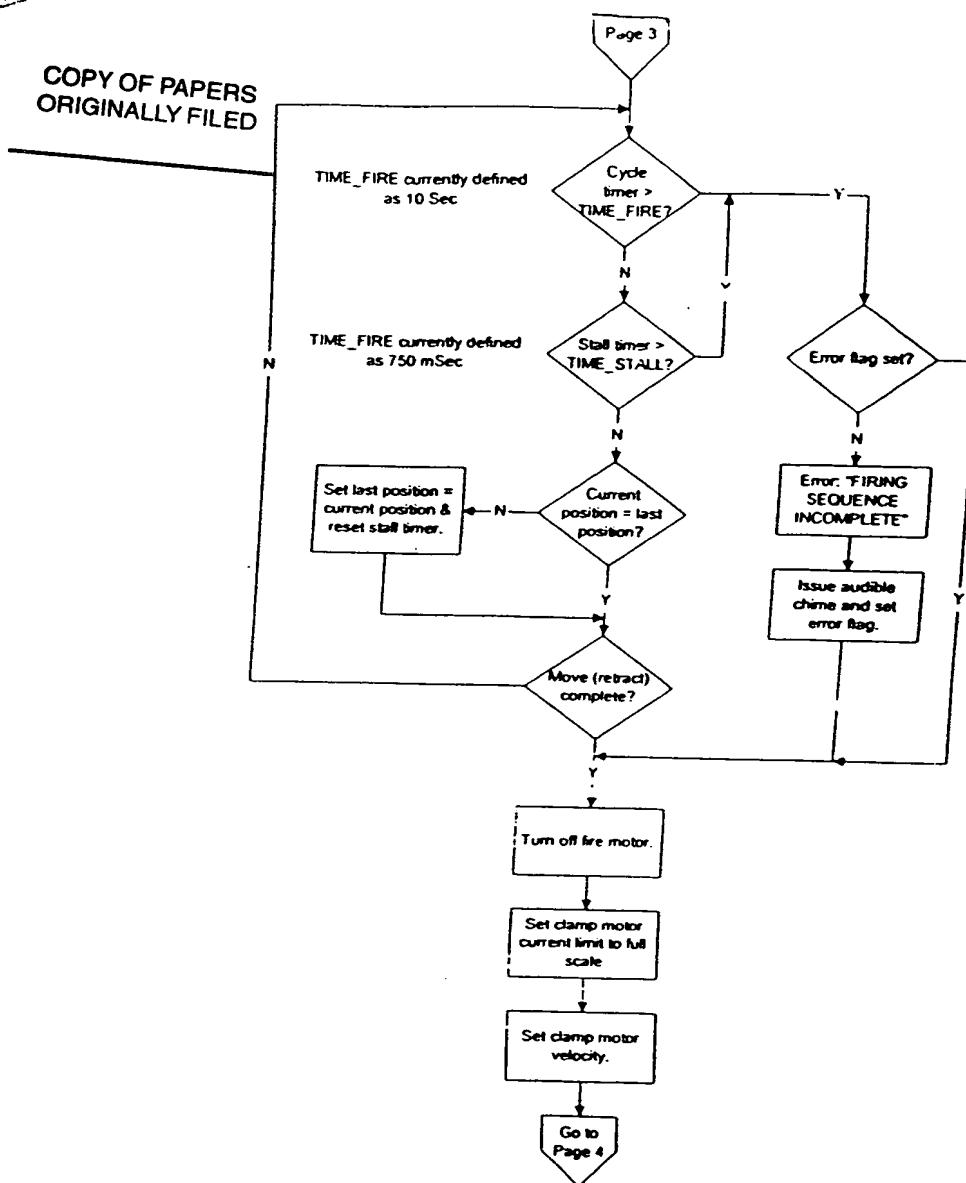


FIG. 21c

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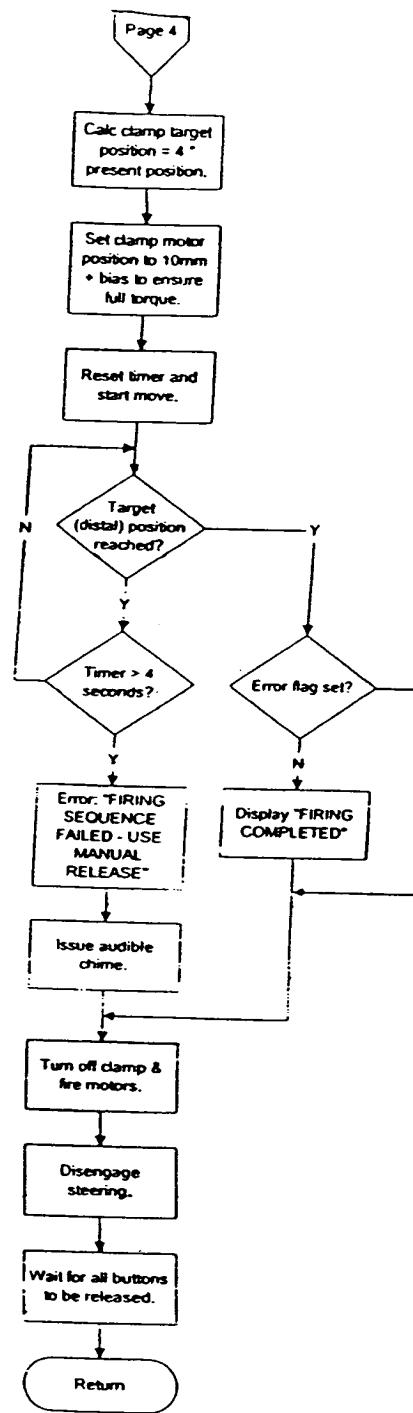


FIG. 21d



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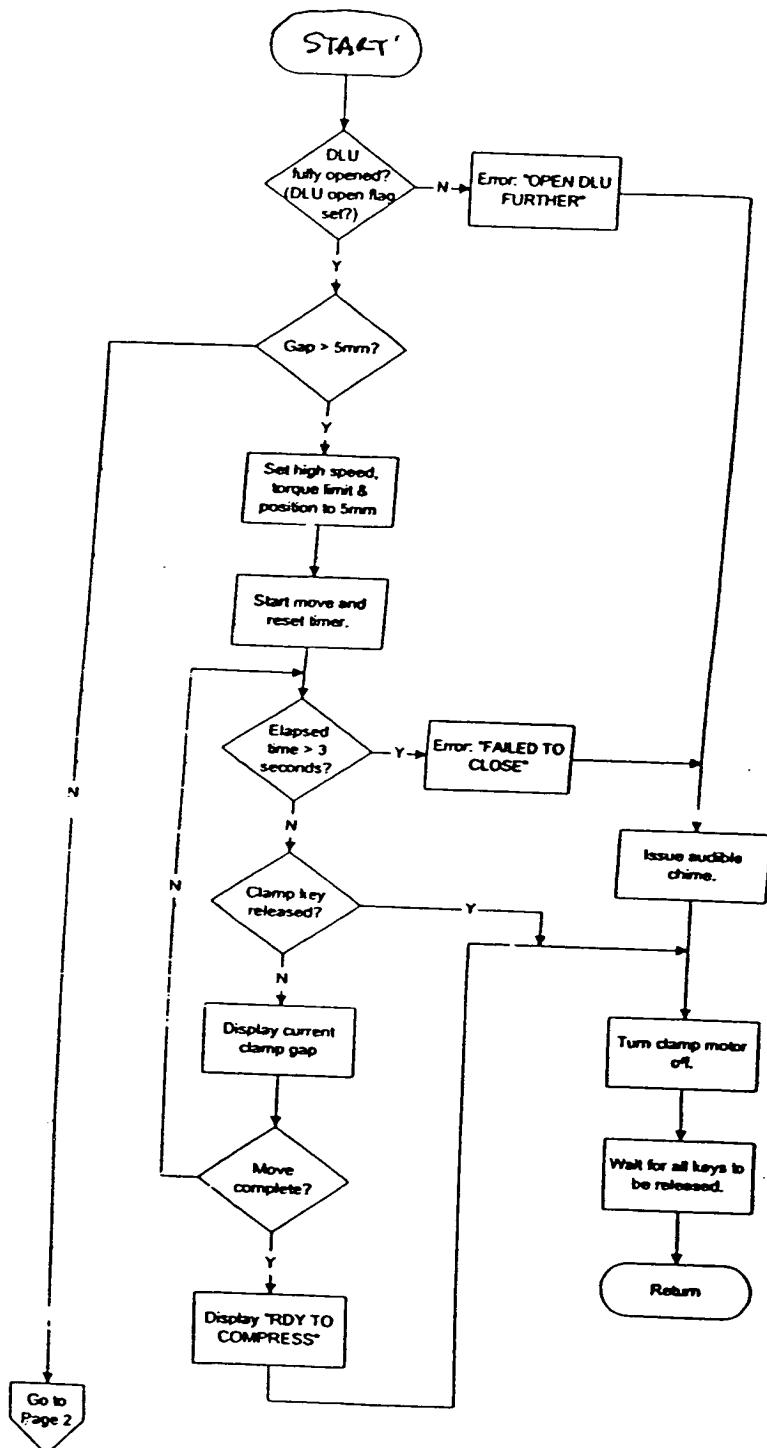


FIG. 22a



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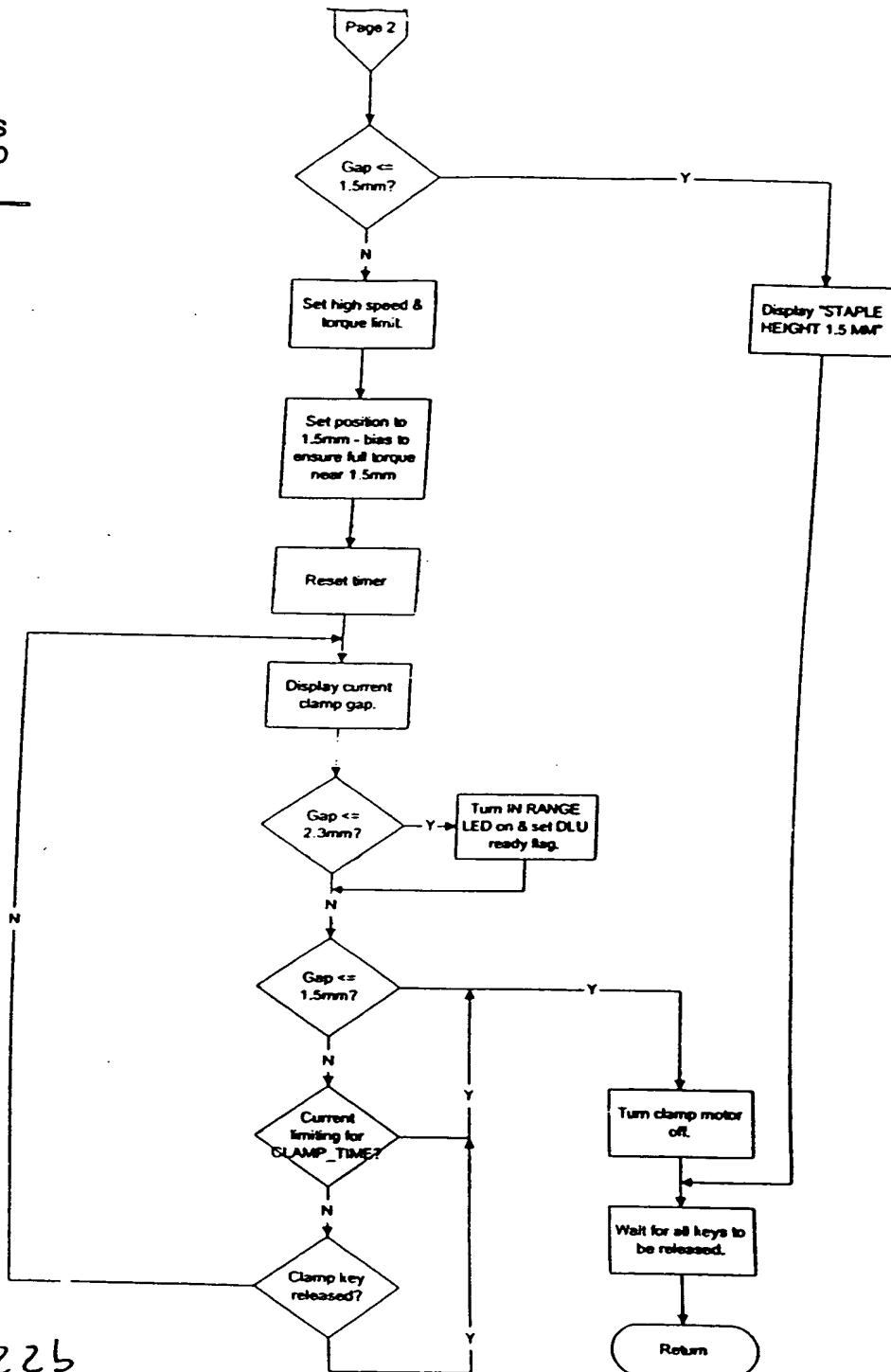


FIG. 225



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*The kernel tries 3x w/ 100mS time
between tries to write DLU.

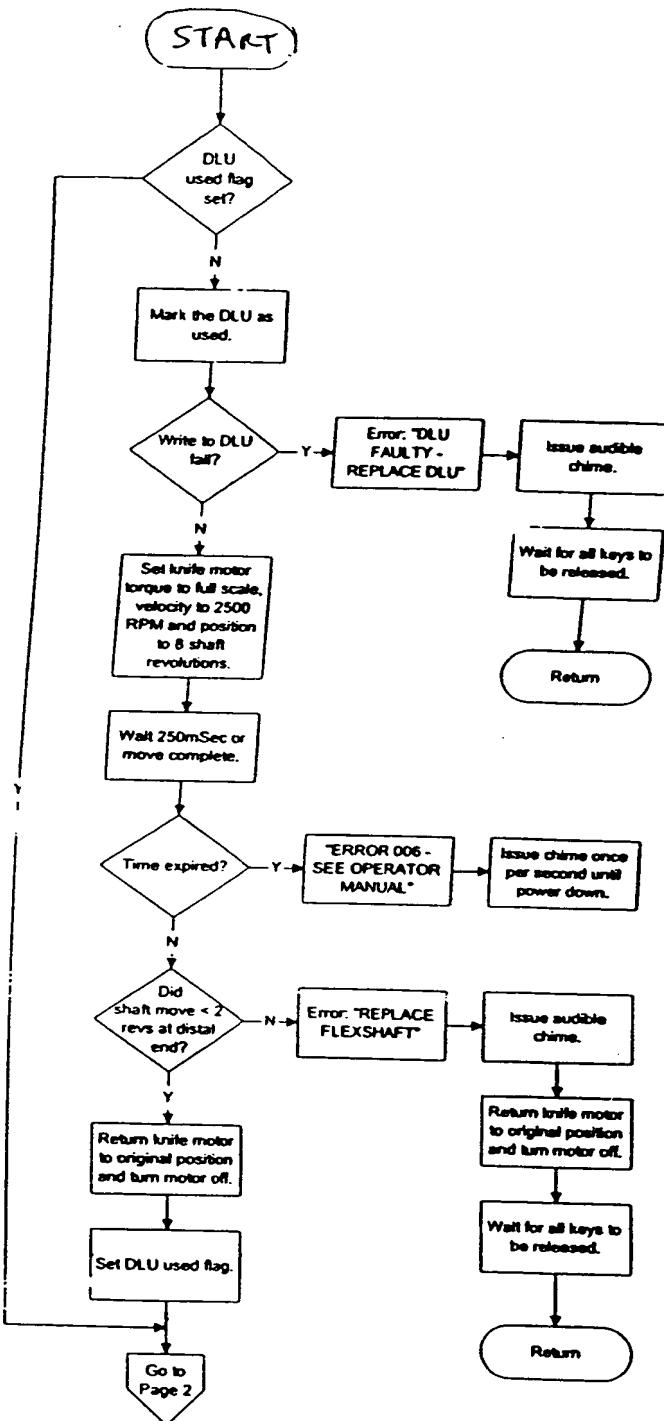


FIG. 23a



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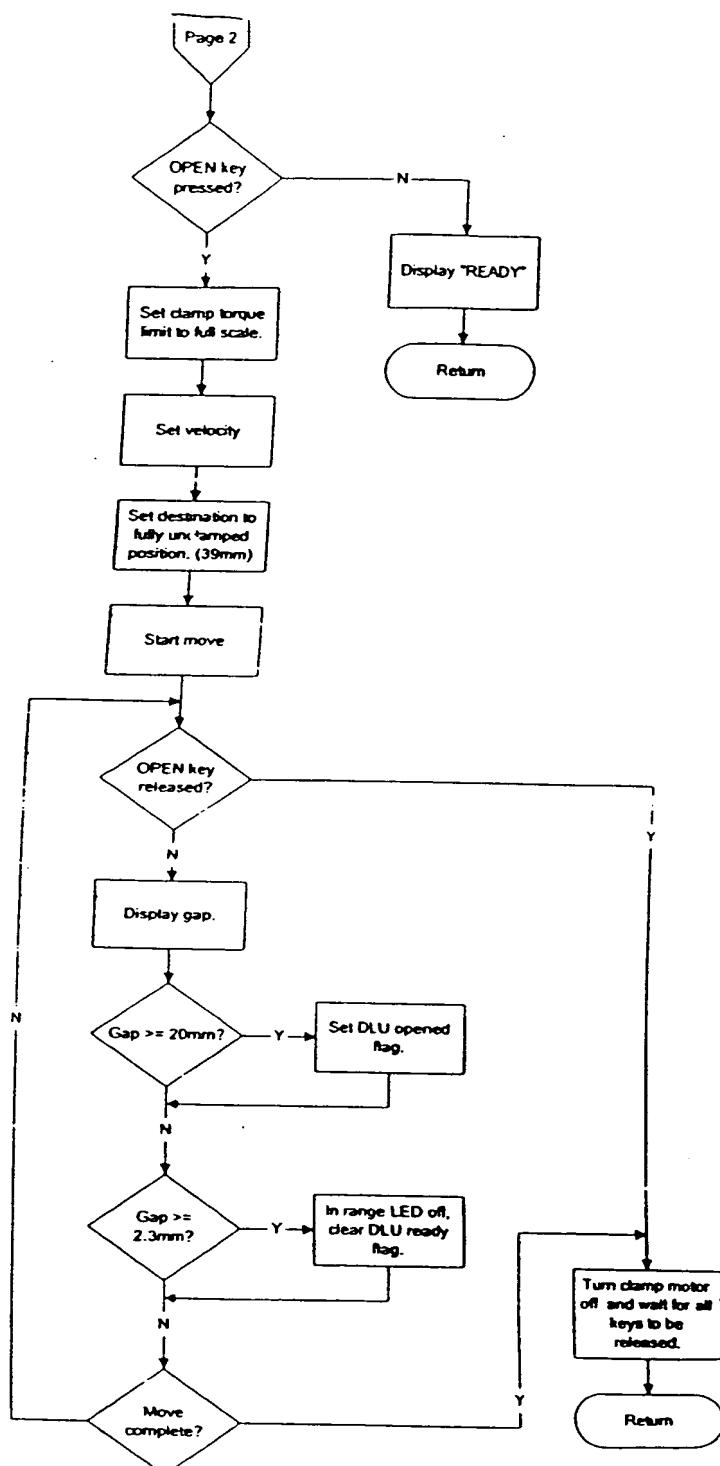


FIG. 23b

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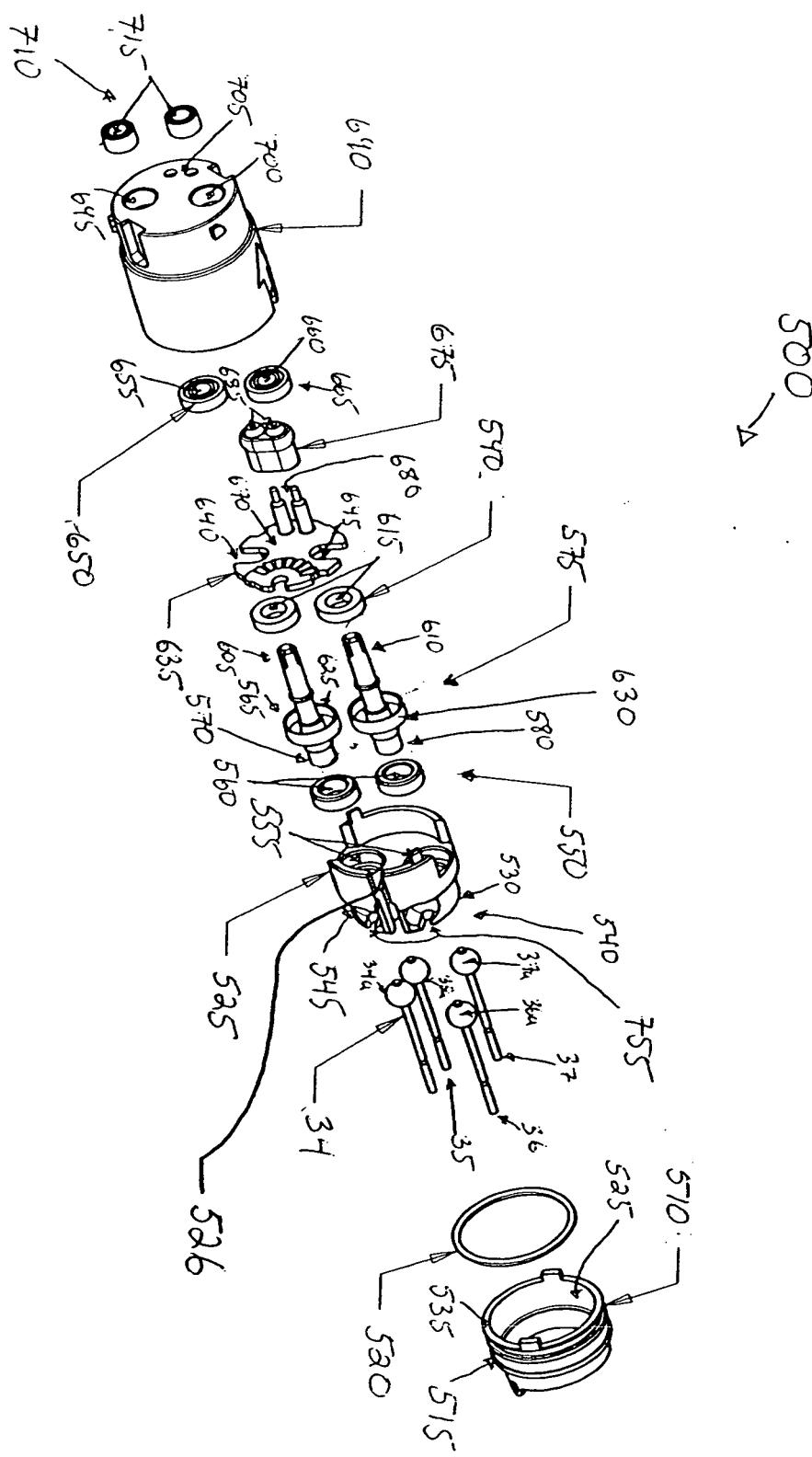
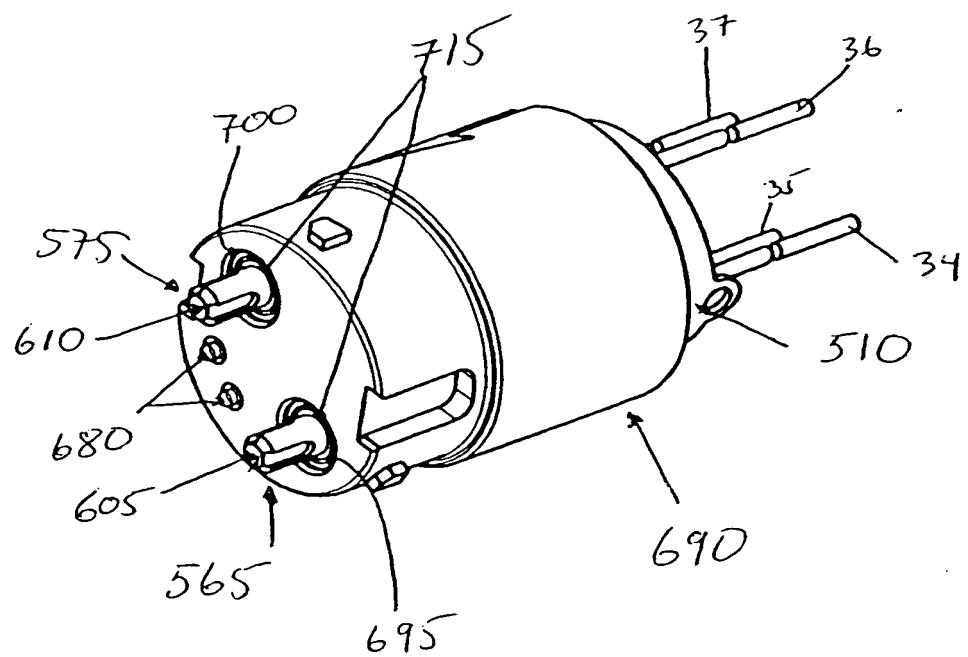


Figure 24a

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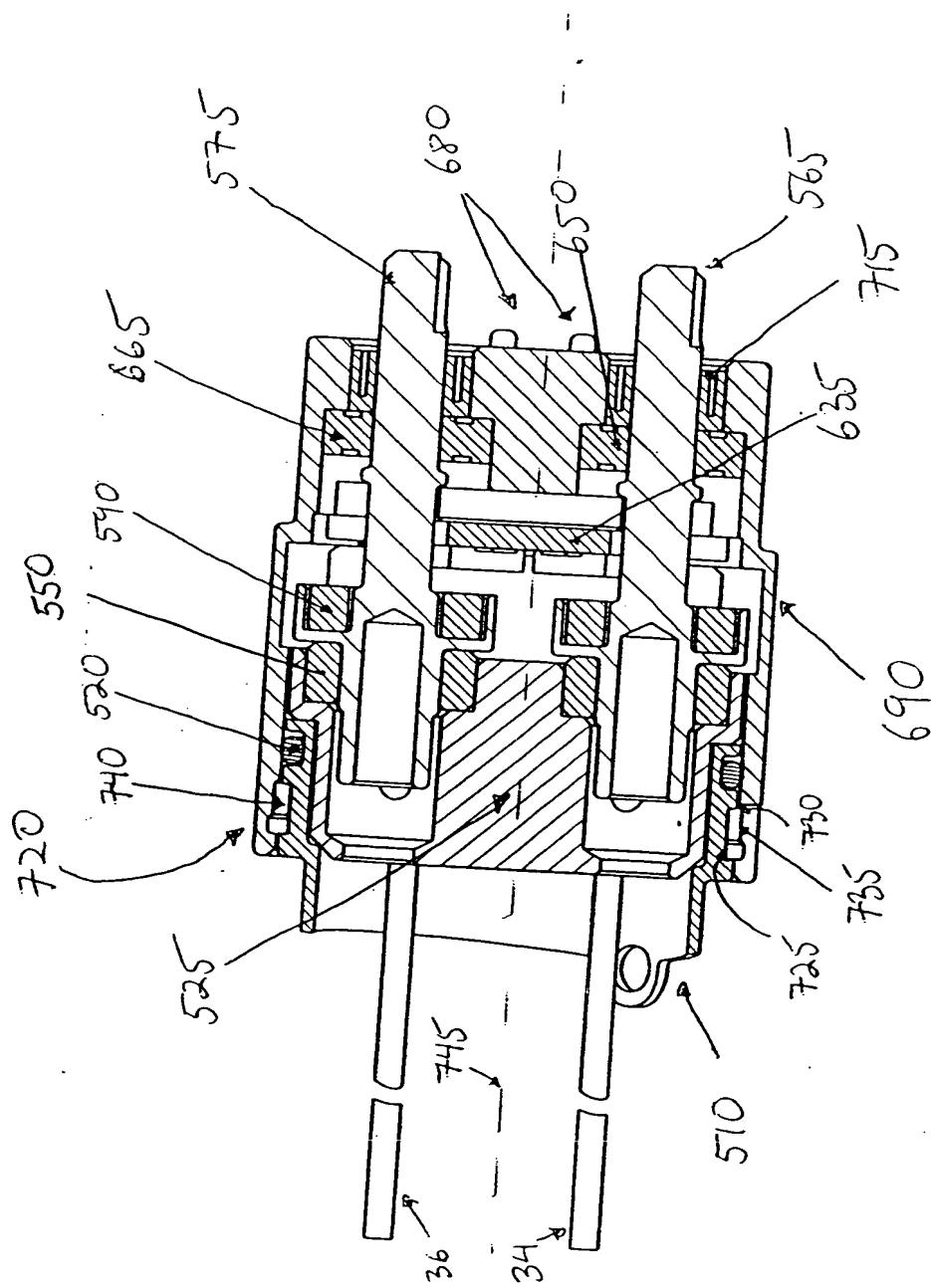
Figure 24b





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Figure 25





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Figure 26a

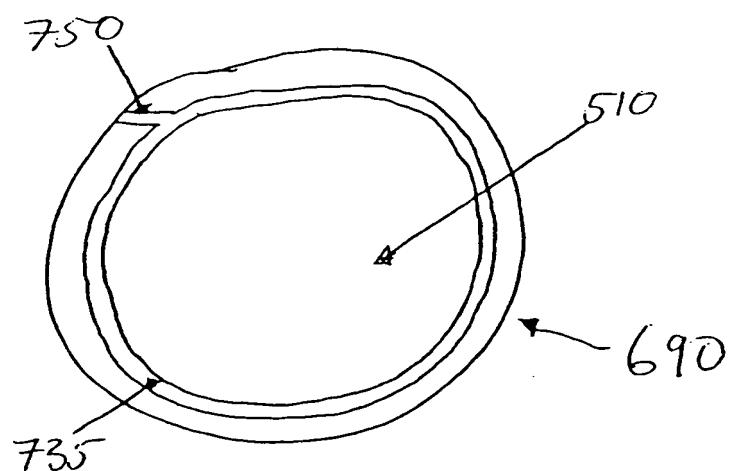
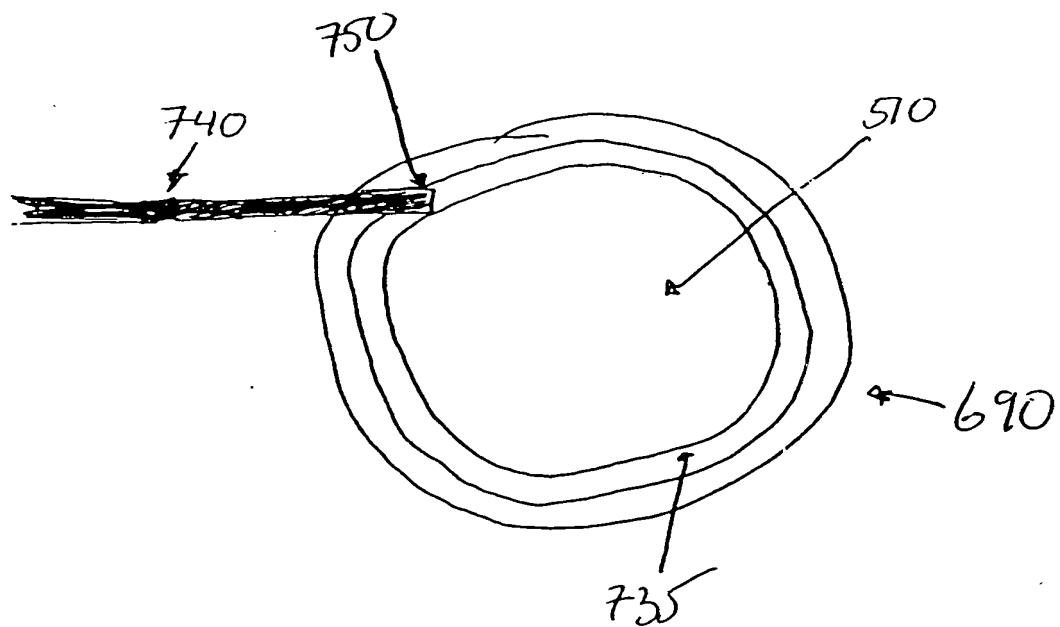
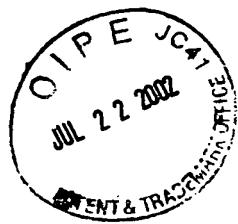


Figure 26b





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Figure 26c

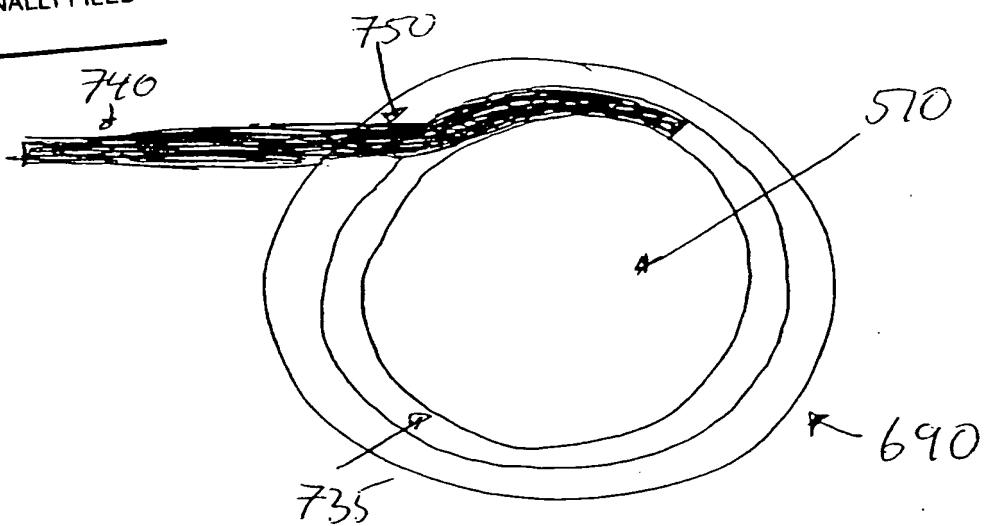
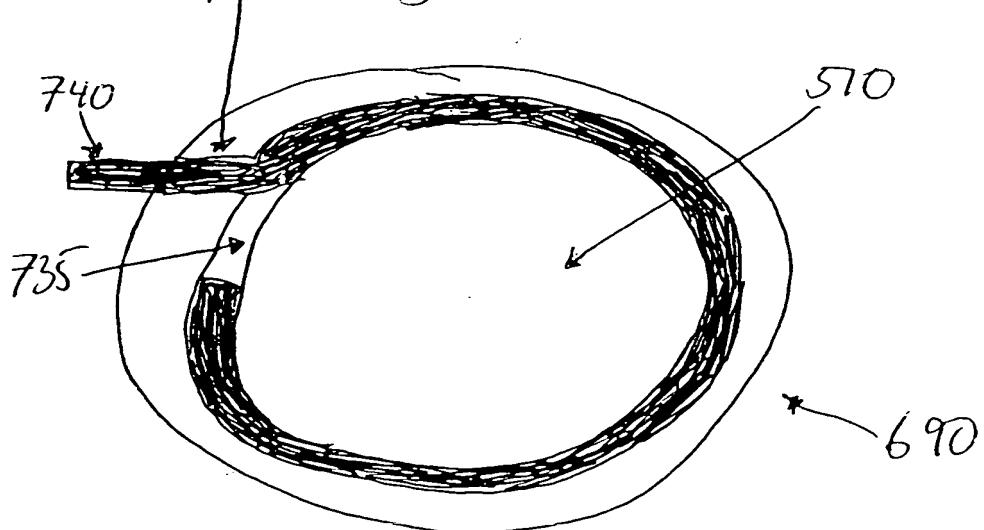
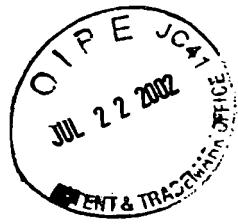
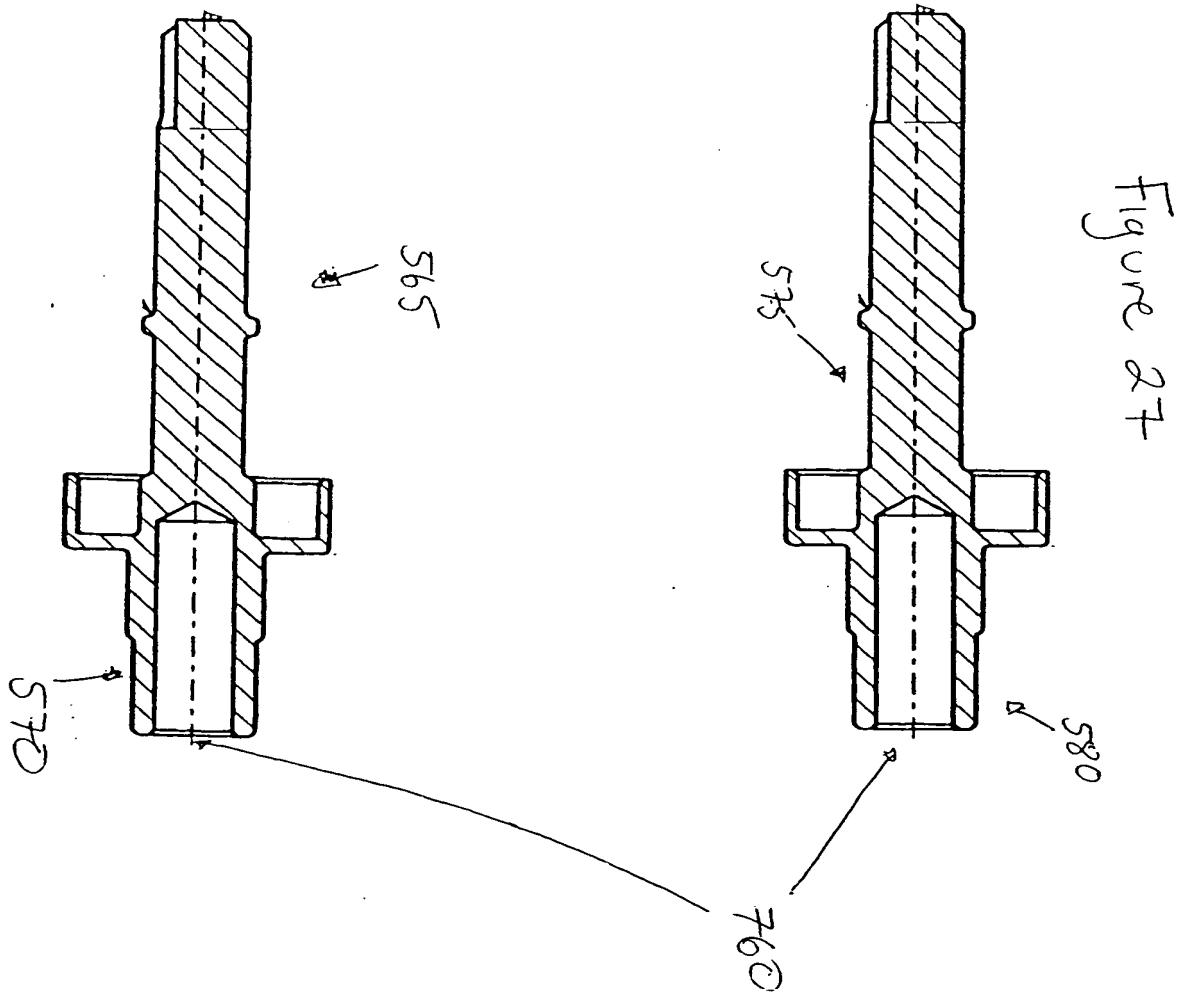


Figure 26d





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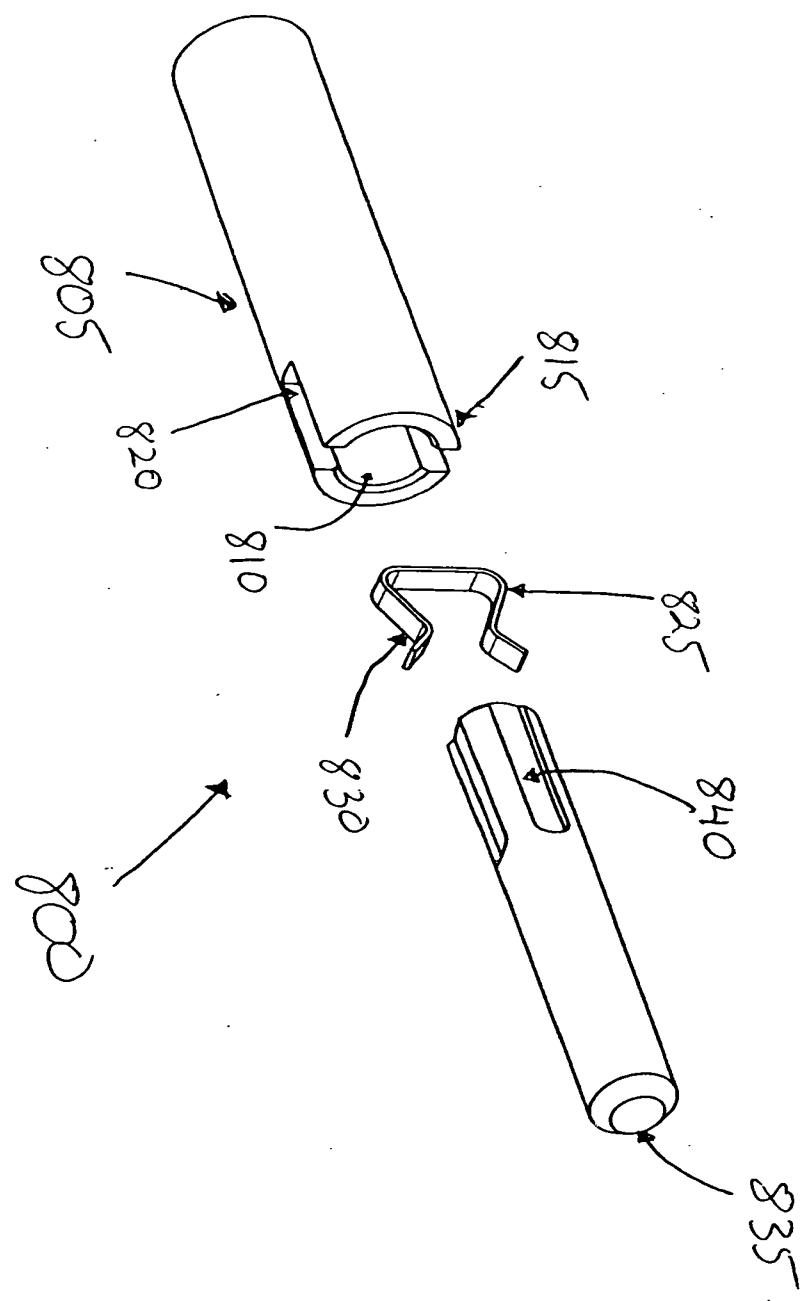


Figure 28a



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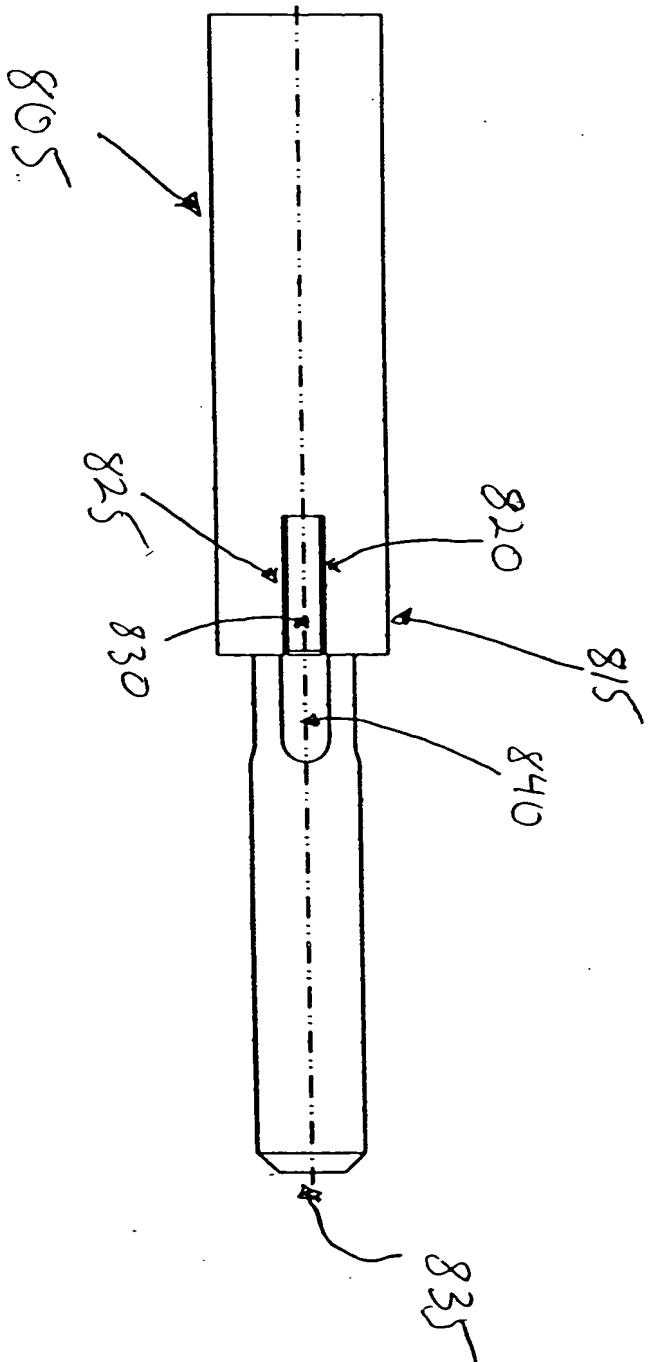


Figure 28b



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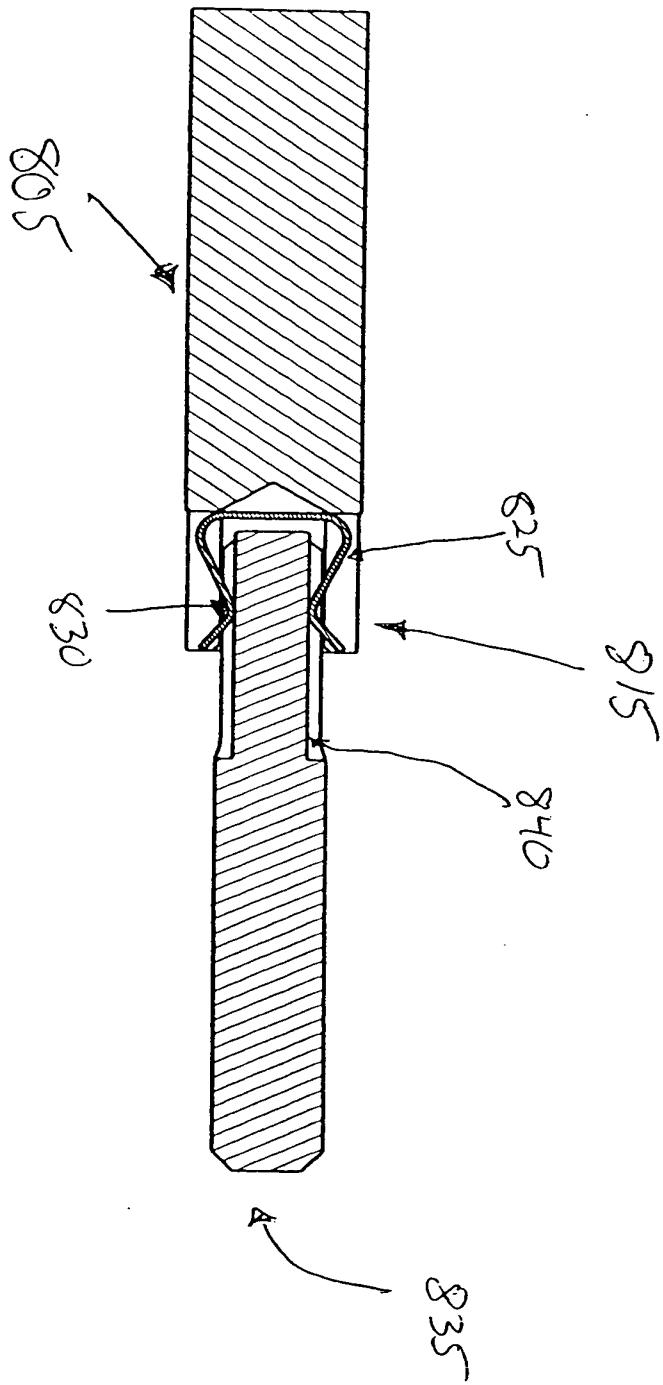


Figure 28C



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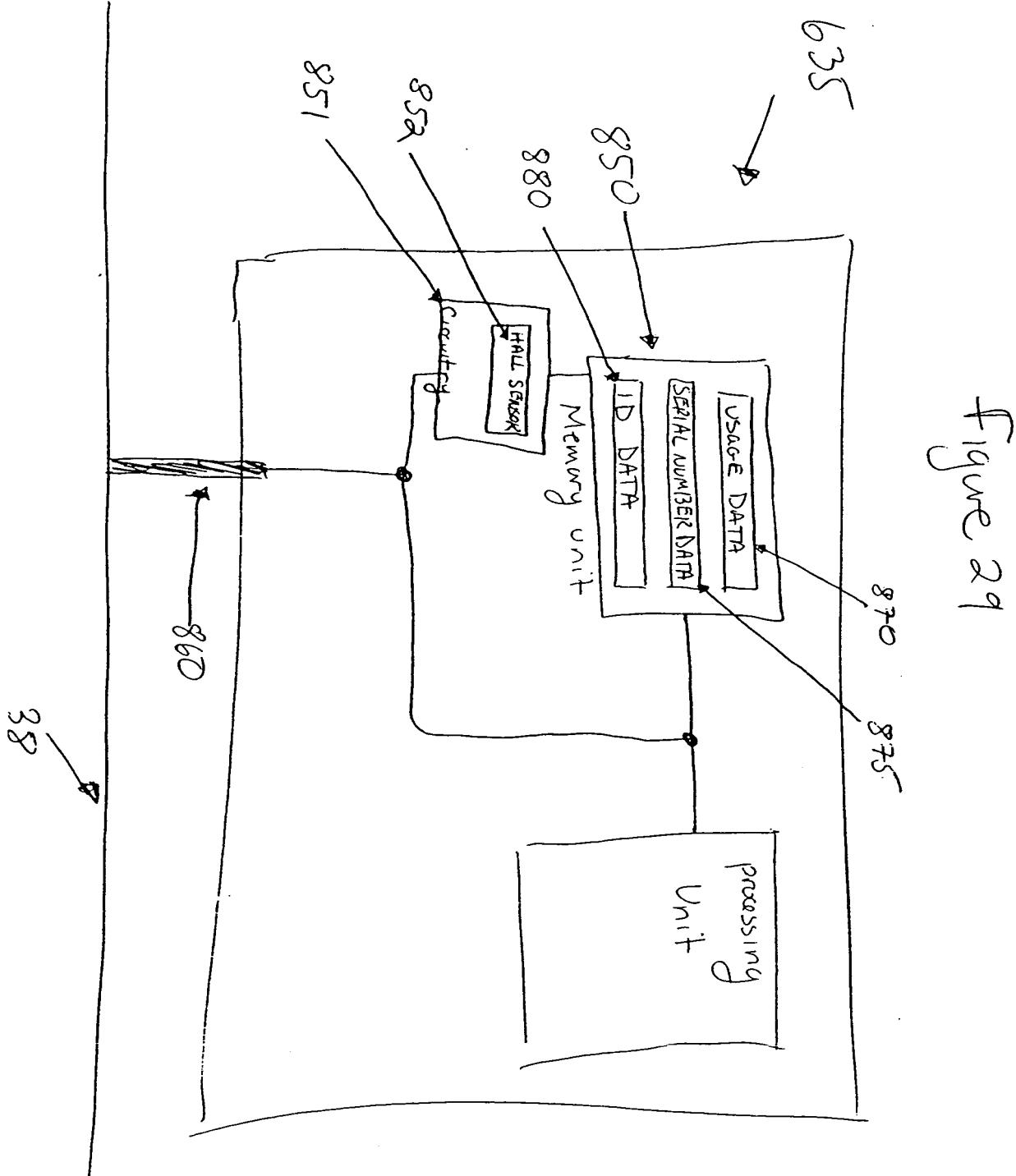


Figure 29



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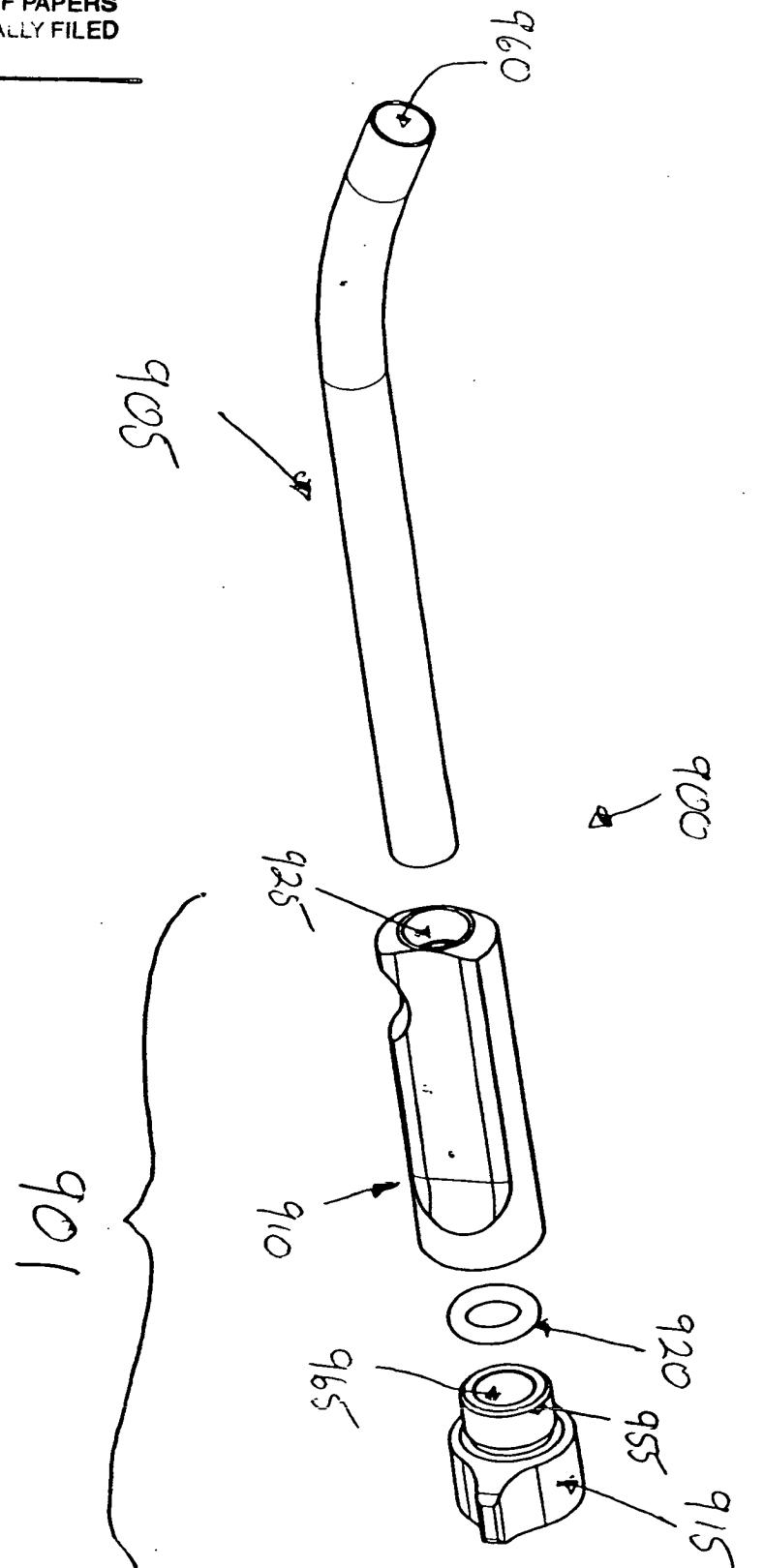


Figure 30a



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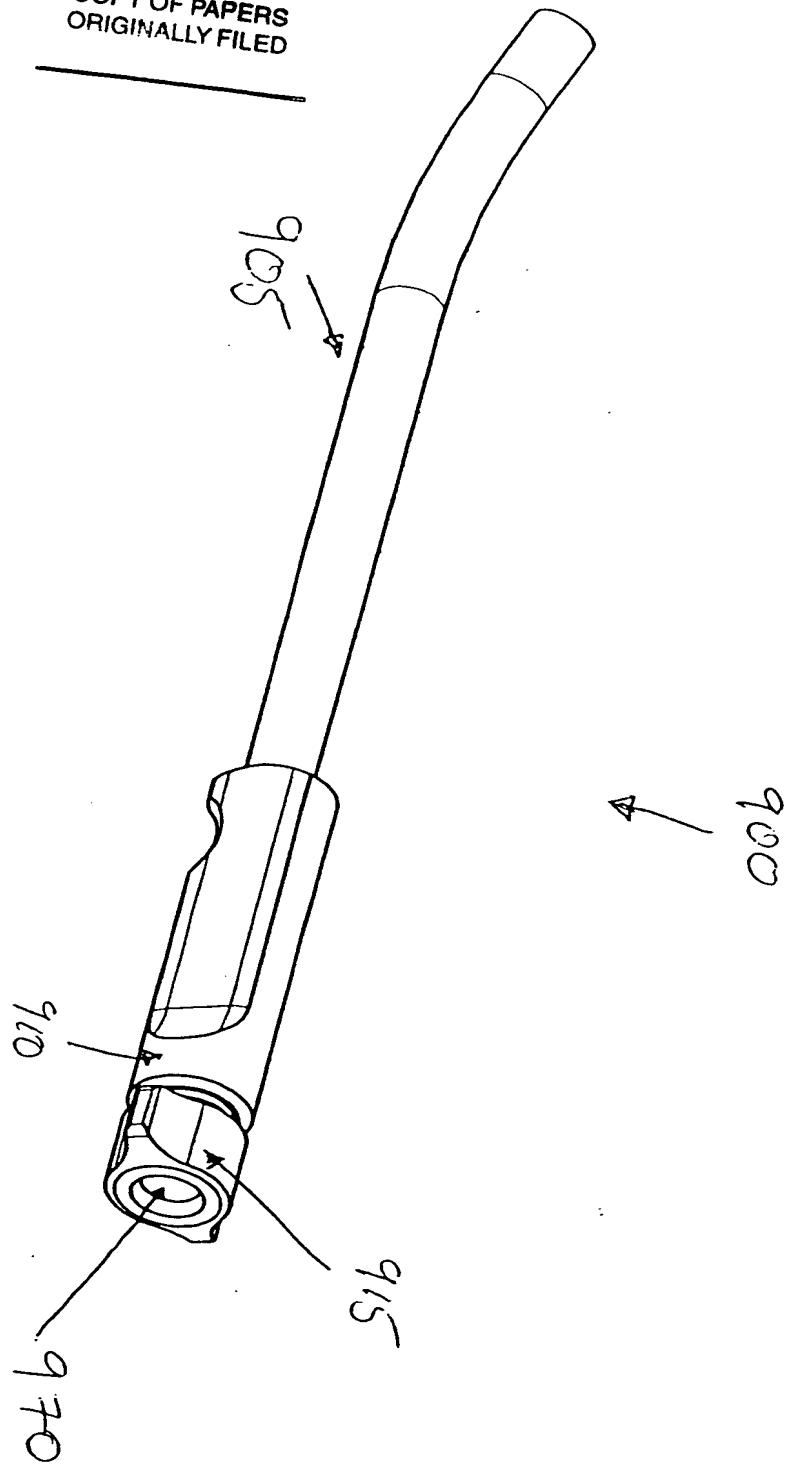
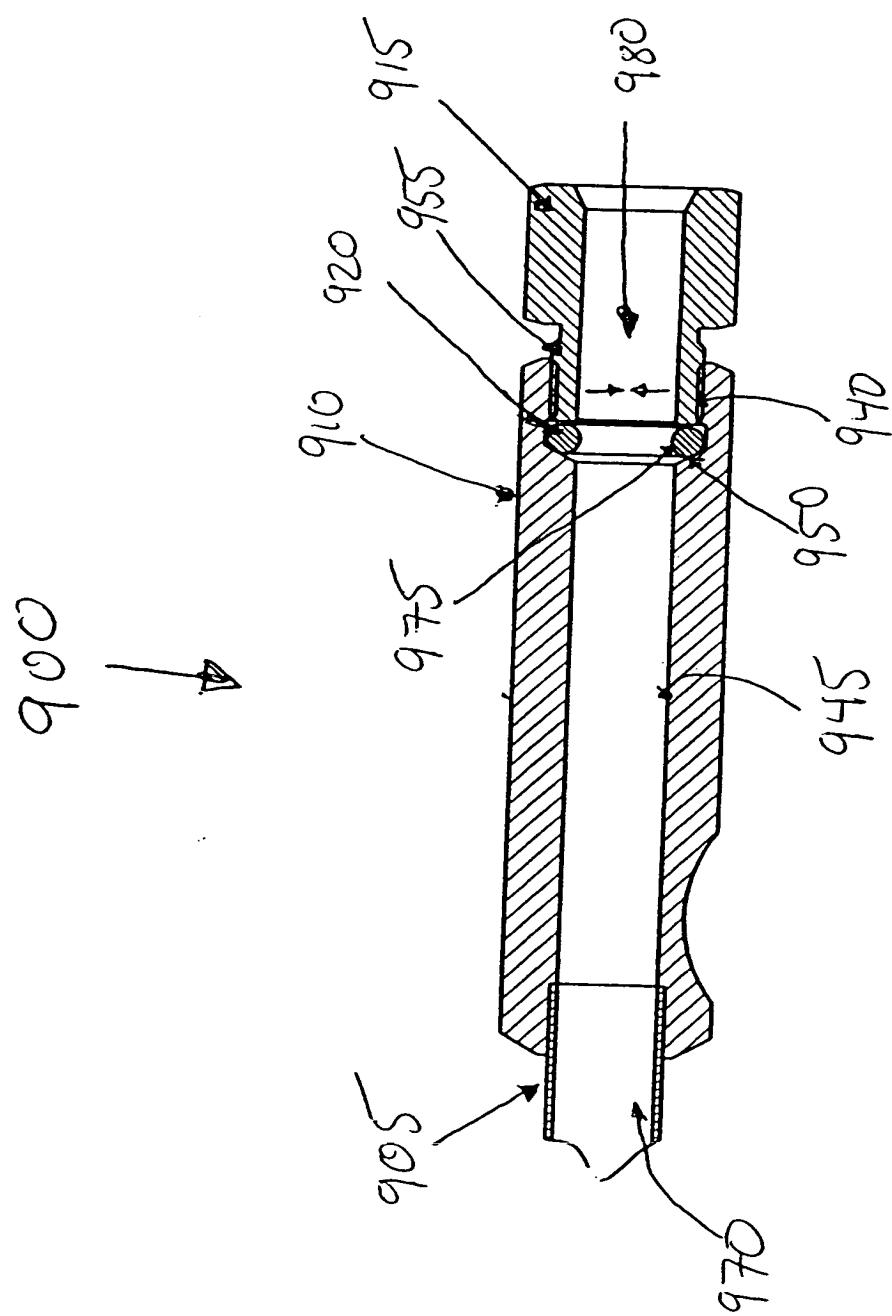


Figure 3D**b**



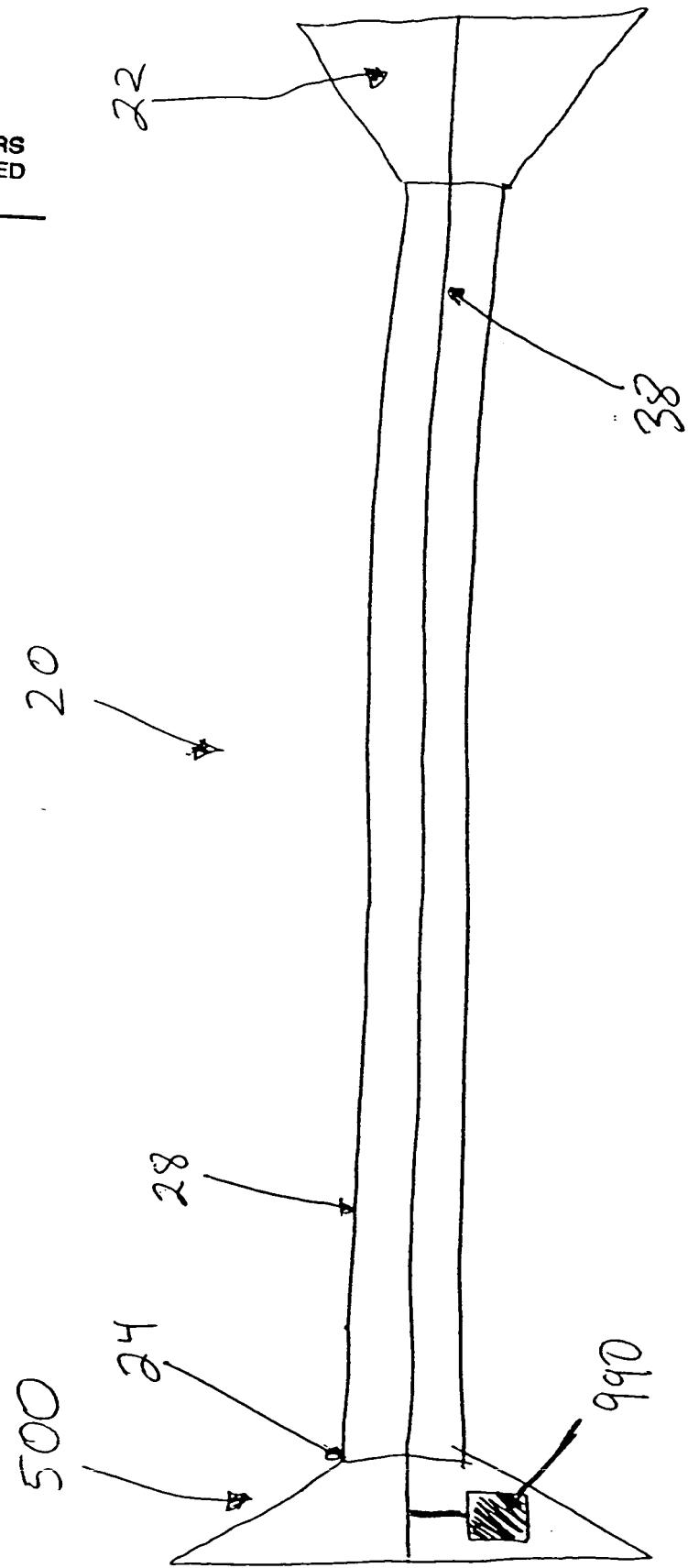
Figure 30C





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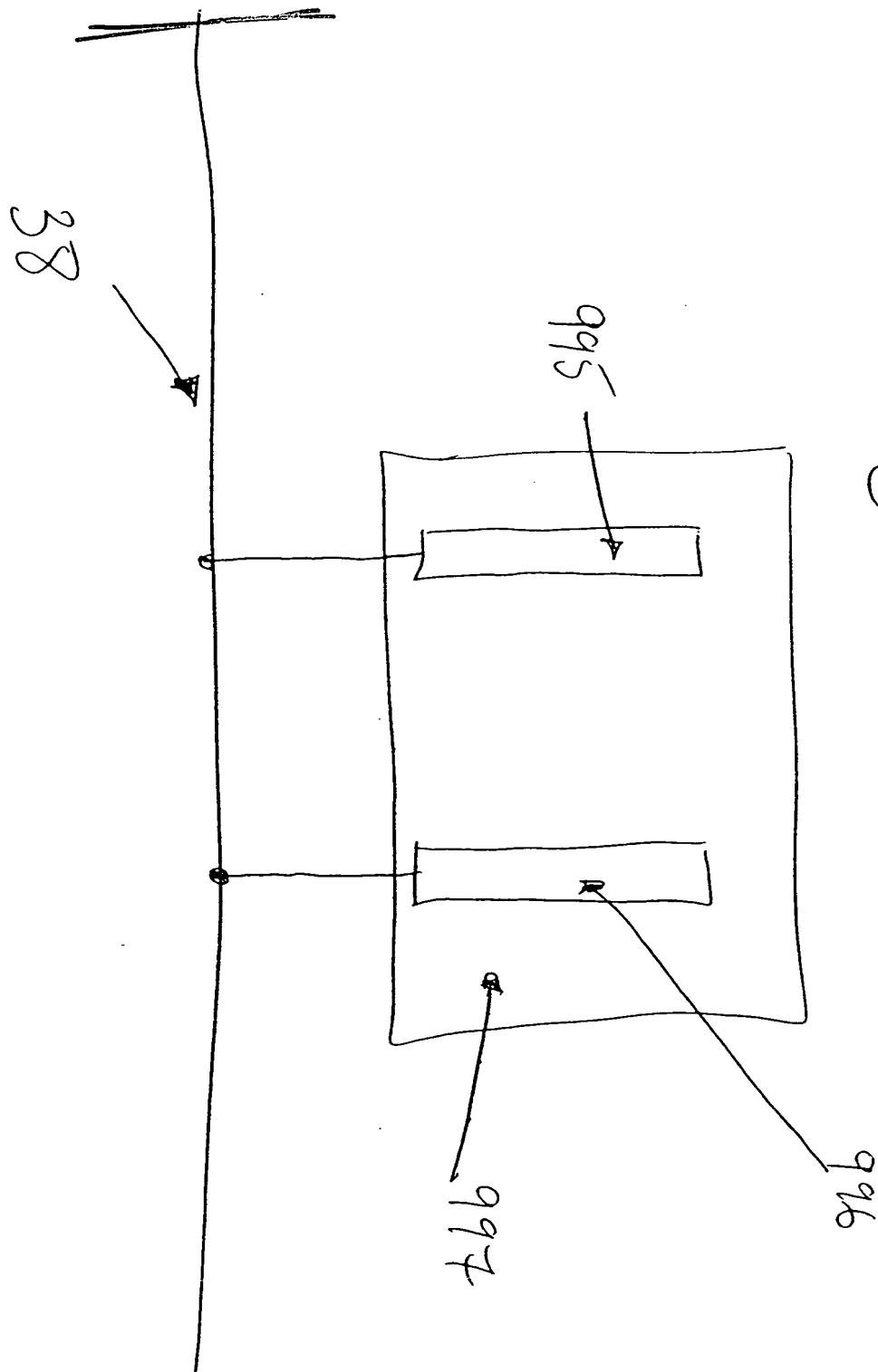


Figure 32